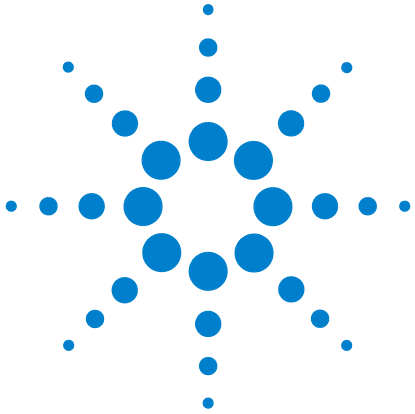

Agilent U7231A DDR3 Compliance Test Application

Compliance Testing Notes

Agilent Technologies

Notices

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DDR3 —An Overview

DDR3 SDRAM or double data rate three synchronous dynamic random access memory is a random access memory technology used for high speed storage of the working data of an electronic device. It is an evolutionary improvement over its predecessor, DDR2 SDRAM.

Table 1 General Characteristics and Specifications of DDR3

Component Speed	Module Speed	Data Rate	Memory Clock
DDR3-800	PC3-6400	800 MT/s	100 MHz (10 ns)
DDR3-1066	PC3-8500	1066 MT/s	133 MHz (7.5 ns)
DDR3-1333	PC3-10600	1333 MT/s	166 MHz (6 ns)
DDR3-1600	PC3-12800	1600 MT/s	200 MHz (5 ns)

The DDR3 components are twice as fast as DDR2 memory products. The main advantages of DDR3 are the higher bandwidth and the increase in performance at low power. The DDR3 SDRAM devices offer data transfer rates up to 1600 Mbps. The supply voltage for the memory technology is being reduced from 1.8 volts for DDR2 to just 1.5 volts for DDR3, which promotes longer battery life. The voltage reduction limits the amount of power that is consumed and heat that is generated in connection with the increase in bandwidth.

DDR3 —Quick Reference

Table 2 DDR3 Cycles and Signals

NOTE: 1 = Single Ended probing; 2 = Differential probing; 3 = 2 x Single Ended probing

TEST	Cycle		Based on Test Definition						Required to Perform on Scope						Opt.
	Read	Write	DQ	DQS	CK	ADD	Ctrl	Data Mask Ctrl	DQ	DQS	CK	ADD	Ctrl	Data Mask Ctrl	CS#
tJIT(per)					√						√[2]				
tJIT(cc)					√						√[2]				
tERR(nper)					√						√[2]				
tCH(avg)					√						√[2]				
tCL(avg)					√						√[2]				
tJIT(duty)					√						√[2]				
tCK(avg)					√						√[2]				
VSWING (MAX)		√	√	√		√	√	√	√[2]	√[2]		√[2]	√[2]	√[2]	
SlewR		√	√	√	√	√	√	√	√[2]	√[2]	√[2]	√[2]	√[2]	√[2]	
SlewF		√	√	√	√	√	√	√	√[2]	√[2]	√[2]	√[2]	√[2]	√[2]	
VIH(ac)		√	√	√	√	√	√	√	√[2]	√[2]	√[2]	√[2]	√[2]	√[2]	
VIH(dc)		√	√	√	√	√	√	√	√[2]	√[2]	√[2]	√[2]	√[2]	√[2]	
VIL(ac)		√	√	√	√	√	√	√	√[2]	√[2]	√[2]	√[2]	√[2]	√[2]	
VIL(dc)		√	√	√	√	√	√	√	√[2]	√[2]	√[2]	√[2]	√[2]	√[2]	
SRQseR		√	√	√	√	√	√	√	√[2]	√[2]	√[2]	√[2]	√[2]	√[2]	
SRQseF		√	√	√	√	√	√	√	√[2]	√[2]	√[2]	√[2]	√[2]	√[2]	
VOH(ac)		√	√	√	√	√	√	√	√[2]	√[2]	√[2]	√[2]	√[2]	√[2]	
VOH(dc)		√	√	√	√	√	√	√	√[2]	√[2]	√[2]	√[2]	√[2]	√[2]	
VOL(ac)		√	√	√	√	√	√	√	√[2]	√[2]	√[2]	√[2]	√[2]	√[2]	
VOL(dc)		√	√	√	√	√	√	√	√[2]	√[2]	√[2]	√[2]	√[2]	√[2]	
AC Overshoot		√	√	√	√	√	√	√	√[2]	√[2]	√[2]	√[2]	√[2]	√[2]	
AC Undershoot		√	√	√	√	√	√	√	√[2]	√[2]	√[2]	√[2]	√[2]	√[2]	
VID(ac)		√		√	√					√[3]	√[3]				
VIX(ac)		√		√	√					√[3]	√[3]				
VOX(ac)		√		√						√[3]					

Table 2 DDR3 Cycles and Signals

NOTE: 1 = Single Ended probing; 2 = Differential probing; 3 = 2 x Single Ended probing

TEST	Cycle		Based on Test Definition						Required to Perform on Scope						Opt.
	Read	Write	DQ	DQS	CK	ADD	Ctrl	Data Mask Ctrl	DQ	DQS	CK	ADD	Ctrl	Data Mask Ctrl	CS#
Eye Diagram - Read	√		√	√					√[2]	√[2]					
Eye Diagram - Write		√	√	√					√[2]	√[2]					
High State Ringing			√	√		√	√	√	√[1, 2]	√[1,2]		√[1,2]	√[1,2]	√[1,2]	
Low State Ringing			√	√		√	√	√	√[1, 2]	√[1,2]		√[1,2]	√[1,2]	√[1,2]	
tDQSCK	√			√	√				√[2]	√[2]	√[2]				√
tHZ(DQ)	√		√		√				√[2]	√[2]	√[2]				√
tLZ(DQS)	√			√	√				√[2]	√[2]	√[2]				√
tLZ(DQ)	√		√		√				√[2]	√[2]	√[2]				√
tDQSQ	√		√	√					√[2]	√[2]	√[2]				√
tQH	√		√	√					√[2]	√[2]	√[2]				√
tDQSS		√		√	√				√[2]	√[2]	√[2]				√
tDQSH	√			√					√[2]	√[2]	√[2]				√
tDQSL	√			√					√[2]	√[2]	√[2]				√
tDSS		√		√	√				√[2]	√[2]	√[2]				√
tDSH		√		√	√				√[2]	√[2]	√[2]				√
tWPST		√		√					√[2]	√[2]	√[2]				√
tWPRE		√		√					√[2]	√[2]	√[2]				√
tRPRE	√			√					√[2]	√[2]	√[2]				√
tRPST	√			√					√[2]	√[2]	√[2]				√
tDS(base)		√	√						√[2]	√[2]	√[2]				√
tDH(base)		√	√						√[2]	√[2]	√[2]				√
tIS(base)	√				√	√	√				√[2]	√[2]	√[2]		√
tIH(base)	√				√	√	√				√[2]	√[2]	√[2]		√

DDR3 Compliance Test Application — At A Glance

The Agilent U7231A DDR3 Compliance Test Application is a DDR3 (Double Data Rate 3) test solution that covers electrical, clock and timing parameters of the JEDEC (Joint Electronic Device Engineering Council) specifications, specifically *JESD79-3*. The software helps you in testing all the un-buffered DDR3 device under test (DUT) compliance, with the Agilent 54850A series and 80000 series Infiniium digital storage oscilloscope.

There are 2 main categories of test modes:

- Compliance Tests - These tests are based on the DDR3 JEDEC compliance specifications and are compared to corresponding compliance test limits.
- Advance Debug Tests - These tests are not based on any compliance specification. The primary use of these tests is to perform signal debugging.

The DDR3 Compliance Test Application:

- Lets you select individual or multiple tests to run.
- Lets you identify the device being tested and its configuration.
- Shows you how to make oscilloscope connections to the device under test.
- Automatically checks for proper oscilloscope configuration.
- Automatically sets up the oscilloscope for each test.
- Allows you to determine the number of trials for each test, with the new multi trial run capability.
- Provides detailed information of each test that has been run. The result of maximum twenty five worst trials can be displayed at any one time.
- Creates a printable HTML report of the tests that have been run.

The minimum number of probes required for the tests are:

- Clock tests - 1 probe.
- Electrical tests - 3 probes.
- Clock Timing tests - 3 probes.
- Advanced Debug tests - 3 probes.

NOTE The tests performed by the DDR3 Compliance Test Application are intended to provide a quick check of the physical layer performance of the DUT. These testing are not replacement for an exhaustive test validation plan.

DDR3 SDRAM electrical, clock and timing test standards and specifications are described in the *JESD79-3* document. For more information, please refer to JEDEC web site at www.jedec.org.

Required Equipment and Software

In order to run the DDR3 automated tests, you need the following equipment and software:

- 54850A series or 80000 series Infiniium Digital Storage Oscilloscope. Agilent recommends using 4 GHz and higher bandwidth oscilloscope.
- Infiniium software revision 05.30 or later.
- U7231A DDR3 Compliance Test Application, version 1.0 and higher.
- RAM reliability test software.
- 1169A, 1168A, 1134A, 1132A or 1131A InfiniiMax probe amplifiers.
- N5381A or E2677A differential solder-in probe head, N5382A or E2675A differential browser probe head, N5425A ZIF probe head or N5426A ZIF tips.
- Any computer motherboard system that supports DDR3 memory.
- Keyboard, qty = 1, (provided with the Agilent Infiniium oscilloscope).
- Mouse, qty = 1, (provided with the Agilent Infiniium oscilloscope).

Below are the required licenses:

- U7231A DDR3 Compliance Test Application license.
- N5414A InfiniiScan software license.
- E2688A Serial Data Analysis and Clock Recovery software license.
- N5404A Deep memory option (optional).

In This Book

This manual describes the tests that are performed by the DDR3 Compliance Test Application in more detail; it contains information from (and refers to) the *JESD79-3*, and it describes how the tests are performed.

- Chapter 1, "Installing the DDR3 Compliance Test Application" shows how to install and license the automated test application software (if it was purchased separately).
- Chapter 2, "Preparing to Take Measurements" shows how to start the DDR3 Compliance Test Application and gives a brief overview of how it is used.
- Chapter 3, "Measurement Clock Tests" describes the measurement clock tests including clock period jitter, clock to clock period jitter, cumulative error, average high and low pulse width, half period jitter and average clock period tests.
- Chapter 4, "Single-Ended Signals AC Input Parameters Tests" shows how to run the single-ended signals AC input parameters tests. This chapter includes input signal maximum peak to peak swing tests, input signal minimum slew rate (rising) tests, input signal minimum slew rate (falling) tests, input logic high tests and input logic low tests.
- Chapter 5, "Single-Ended Signals AC Output Parameters Tests" shows how to run the single-ended signals AC output parameters tests.
- Chapter 6, "Single-Ended Signals Overshoot/Undershoot Tests" describes the AC overshoot and undershoot tests probing and method of implementation.
- Chapter 7, "Differential Signals AC Input Parameters Tests" describes the V_{ID} AC differential input voltage tests and V_{IX} AC differential cross point voltage tests.
- Chapter 8, "Differential Signal AC Output Parameters Tests" contains more information on the V_{OX} AC differential cross point voltage tests.
- Chapter 9, "Clock Timing (CT) Tests" describes the clock timing operating conditions of DDR3 SDRAM as defined in the specification.
- Chapter 10, "Data Strobe Timing (DST) Tests" describes various data strobe timing tests including tHZ(DQ), tLZ(DQS), tLZ(DQ), tDQSQ, tQH, tDQSS, tDQSH, tDQSL, tDSS, tDSH, tWPST, tWPRE, tRPRE and tRPST tests.
- Chapter 11, "Data Mask Timing (DMT) Tests" describes the data mask timing tests including tDS(base) and tDH(base) tests.
- Chapter 12, "Command and Address Timing (CAT) Tests" describes the command and address timing tests including address and control input setup time as well as address and control input hold time.

- Chapter 13, “Advanced Debug Mode Read-Write Eye-Diagram Tests” describes the user defined real-time eye-diagram test for read cycle and write cycle.
- Chapter 14, “Advance Debug Mode High-Low State Ringing Tests” shows the high state and low state ringing test method of implementation.
- Chapter 15, “Calibrating the Infiniium Oscilloscope and Probe” describes how to calibrate the oscilloscope in preparation for running the DDR3 automated tests.
- Chapter 16, “InfiniiMax Probing” describes the probe amplifier and probe head recommendations for DDR3 testing.
- Chapter 17, “Common Error Messages” describes the error dialog boxes that can appear and how to remedy the problem.

See Also

- The DDR3 Compliance Test Application’s online help, which describes:
  - Starting the DDR3 compliance test application.
  - Creating or opening a test project.
  - Setting up DDR3 test environment.
  - Selecting tests.
  - Configuring selected tests.
  - Connecting the oscilloscope to the DUT.
  - Running tests.
  - Viewing test results.
  - Viewing/printing the HTML test report.
  - Understanding the HTML report.
  - Saving test projects.

Contact Agilent

For more information on DDR3 Compliance Test Application or other Agilent Technologies' products, applications and services, please contact your local Agilent office. The complete list is available at:

www.agilent.com/find/contactus

Phone or Fax

United States:

(tel) 800 829 4444

(fax) 800 829 4433

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(tel) 877 894 4414

(fax) 800 746 4866

China:

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(fax) 800 820 2816

Europe:

(tel) 31 20 547 2111

Japan:

(tel) (81) 426 56 7832

(fax) (81) 426 56 7840

Korea:

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Contents

4 Single-Ended Signals AC Input Parameters Tests

1 Installing the DDR3 Compliance Test Application

If you purchased the U7231A DDR3 Compliance Test Application separately, you need to install the software and license key.

Installing the Software

1 Make sure you have version 05.30 or higher of the Infiniium oscilloscope software by choosing **Help>About Infiniium...** from the main menu.

2 To obtain the DDR3 Compliance Test Application, go to Agilent website: http://www.agilent.com/find/U7231A.

3 The link for DDR3 Compliance Test Application will appear. Double-click on it and follow the instructions to download and install the application software.

Installing the License Key

1 Request a license code from Agilent by following the instructions on the Entitlement Certificate.

You will need the oscilloscope's "Option ID Number", which you can find in the **Help>About Infiniium...** dialog box.

2 After you receive your license code from Agilent, choose **Utilities>Install Option License...**.

3 In the Install Option License dialog, enter your license code and click **Install License**.

4 Click **OK** in the dialog that tells you to restart the Infiniium oscilloscope application software to complete the license installation.

5 Click **Close** to close the Install Option License dialog.

6 Choose **File>Exit**.

7 Restart the Infiniium oscilloscope application software to complete the license installation.

2 Preparing to Take Measurements

Before running the DDR3 automated tests, you should calibrate the oscilloscope and probe. No test fixture is required for this DDR3 application. After the oscilloscope and probe have been calibrated, you are ready to start the DDR3 Compliance Test Application and perform the measurements.

Calibrating the Oscilloscope

If you haven't already calibrated the oscilloscope and probe, see Chapter 15, "Calibrating the Infiniium Oscilloscope and Probe".

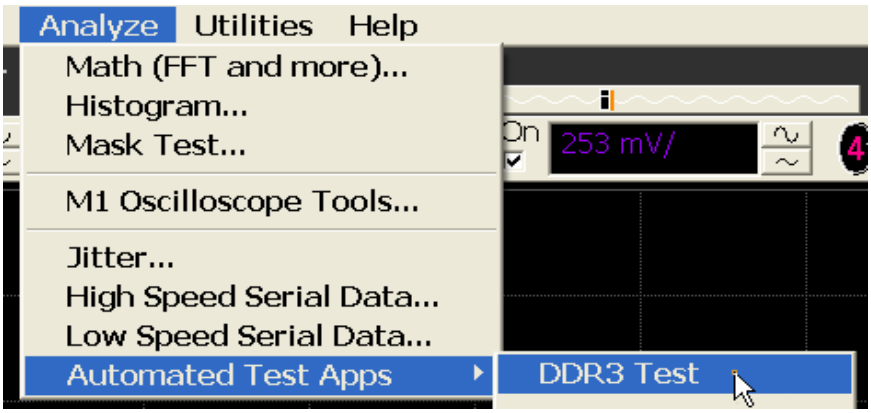
NOTE If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the Utilities>Calibration menu.

NOTE If you switch cables between channels or other oscilloscopes, it is necessary to perform cable and probe calibration again. Agilent recommends that, once calibration is performed, you label the cables with the channel on which they were calibrated.

Starting the DDR3 Compliance Test Application

1 Ensure that the RAM reliability test software is running in the computer system where the Device Under Test (DUT) is attached. This software performs tests to all unused RAM in the system by producing a repetitive burst of read-write data signals to the DDR3 memory.

2 To start the DDR3 Compliance Test Application: From the Infiniium oscilloscope's main menu, choose **Analyze>Automated Test Apps>DDR3 Test**.



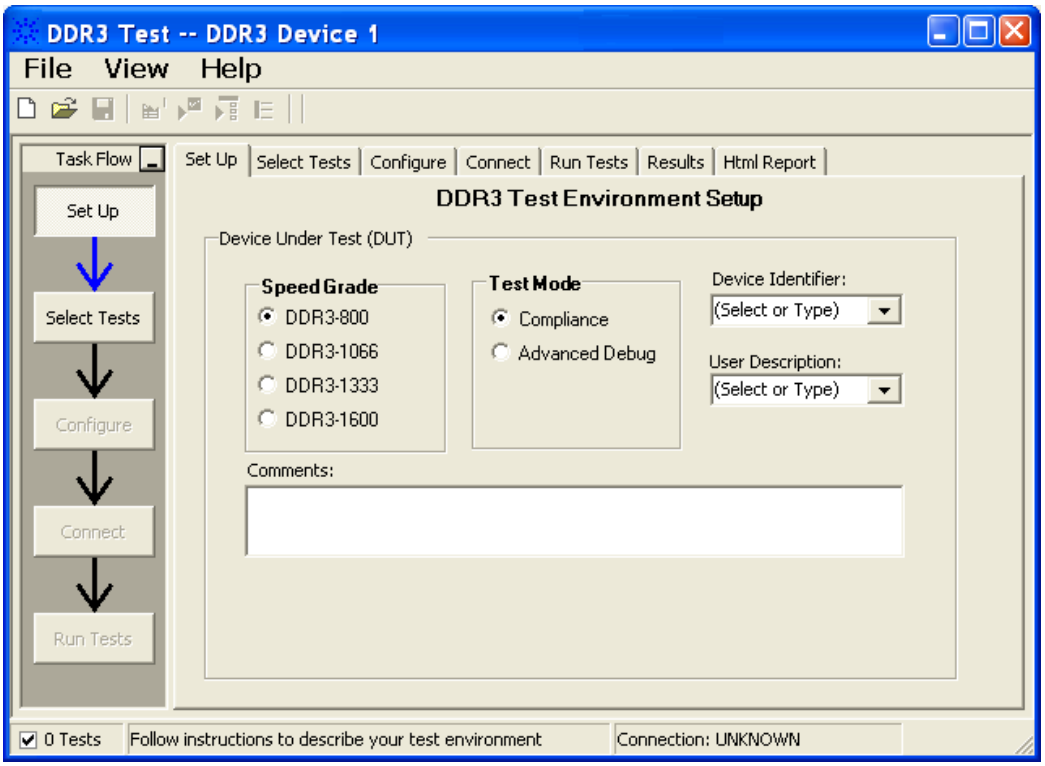


Figure 1 The DDR3 Compliance Test Application

NOTE If DDR3 Test does not appear in the Automated Test Apps menu, the DDR3 Compliance Test Application has not been installed (see Chapter 1, "Installing the DDR3 Compliance Test Application").

Figure 1 shows the DDR3 Compliance Test Application main window. The task flow pane, and the tabs in the main pane, show the steps you take in running the automated tests:

Set Up	Lets you identify and setup the test environment, including information about the device under test.
Select Tests	Lets you select the tests you want to run. The tests are organized hierarchically so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups.
Configure	Lets you configure test parameters (like memory depth). This information appears in the HTML report.
Connect	Shows you how to connect the oscilloscope to the device under test for the tests to be run.
Run Tests	Starts the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing.
Results	Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear.
HTML Report	Shows a compliance test report that can be printed.

NOTE When you close the DDR3 application, each channel's probe is configured as single-ended or differential depending on the last DDR3 test that was run.

Online Help Topics

For information on using the DDR3 Compliance Test Application, see its online help (which you can access by choosing Help>Contents... from the application's main menu).

The DDR3 Compliance Test Application's online help describes:

- Starting the DDR3 Automated Test Application.
  - To view or minimize the task flow pane.
  - To view or hide the toolbar.
- Creating or opening a test project.
- Setting up DDR3 test environment.
- Selecting tests.
- Configuring selected tests.
- Connecting the oscilloscope to the Device Under Test (DUT).
- Running tests.
- Viewing test results.
  - To show reference images and flash mask hits.
  - To change margin thresholds.
- Viewing/printing the HTML test report.
- Understanding the HTML report.
- Saving test projects.

3 Measurement Clock Tests

This section provides the Methods of Implementation (MOIs) for Rising Edge and Pulse Measurements Clock tests using an Agilent 54850A series or 80000 series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR3 Compliance Test Application.

Probing for Measurement Clock Tests

When performing the Measurement Clock tests, the DDR3 Compliance Test Application will prompt you to make the proper connections. The connections for Rising Edge and Pulse Measurement Clock tests may look similar to the following diagram. Refer to the Connection tab in DDR3 Electrical Performance Compliance application for the exact number of probe connections.

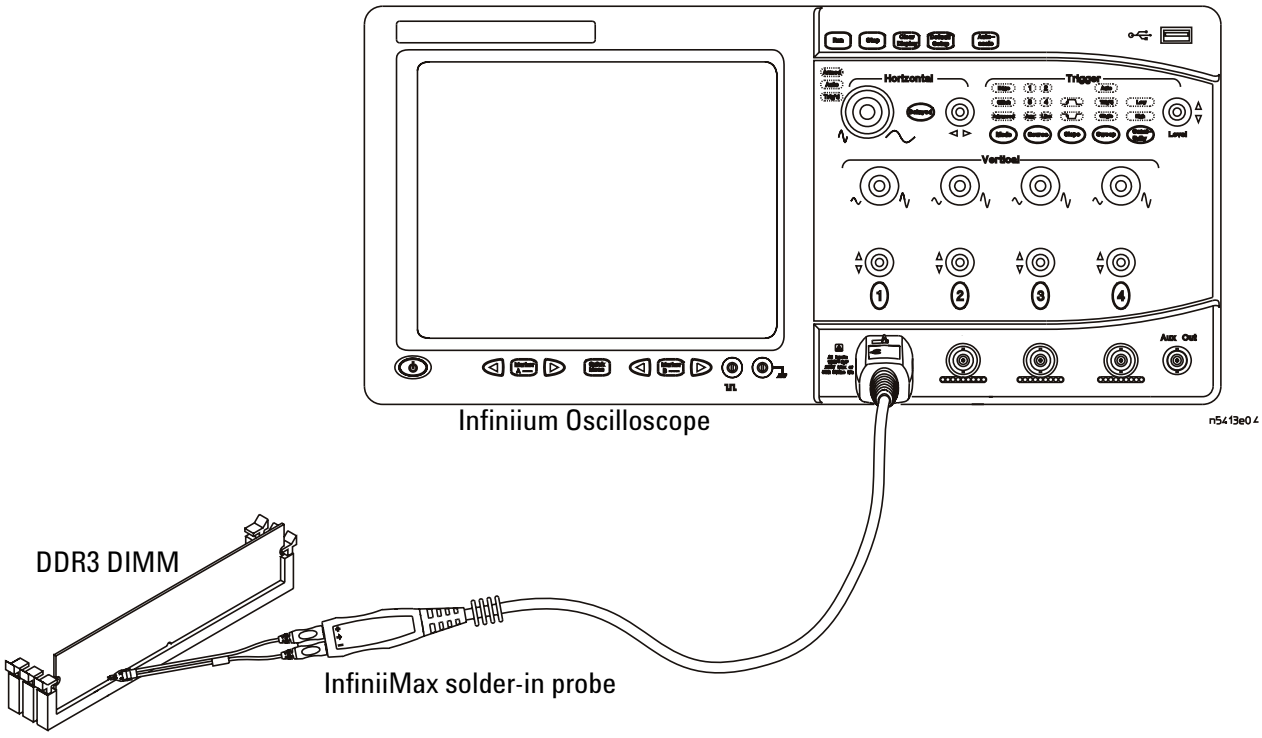


Figure 2 Probing for Measurement Clock Tests

You can use any of the oscilloscope channels as the Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR3 Compliance Test Application. (The channel shown in Figure 2 is just an example.)

For more information on the probe amplifiers and differential probe heads, see Chapter 16, “InfiniiMax Probing,” starting on page 261.

Test Procedure

1. Start the automated test application as described in “Starting the DDR3 Compliance Test Application" on page 27.
2. Ensure that the RAM reliability test software is running on the computer system where the DDR3 Device Under Test (DUT) is attached. This software will perform a test on all the unused RAM on the system by producing a repetitive burst of read-write data signals to the DDR3 memory.
3. Connect the differential solder-in probe head to the PUT on the DDR3 DIMM.
4. Connect the oscilloscope probes to any of the oscilloscope channels.
5. In the DDR3 Test application, click the Set Up tab.
6. Select the Speed Grade options. For the DDR3 Measurement Clock tests, you can select any Speed Grade option.
7. Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.
8. Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

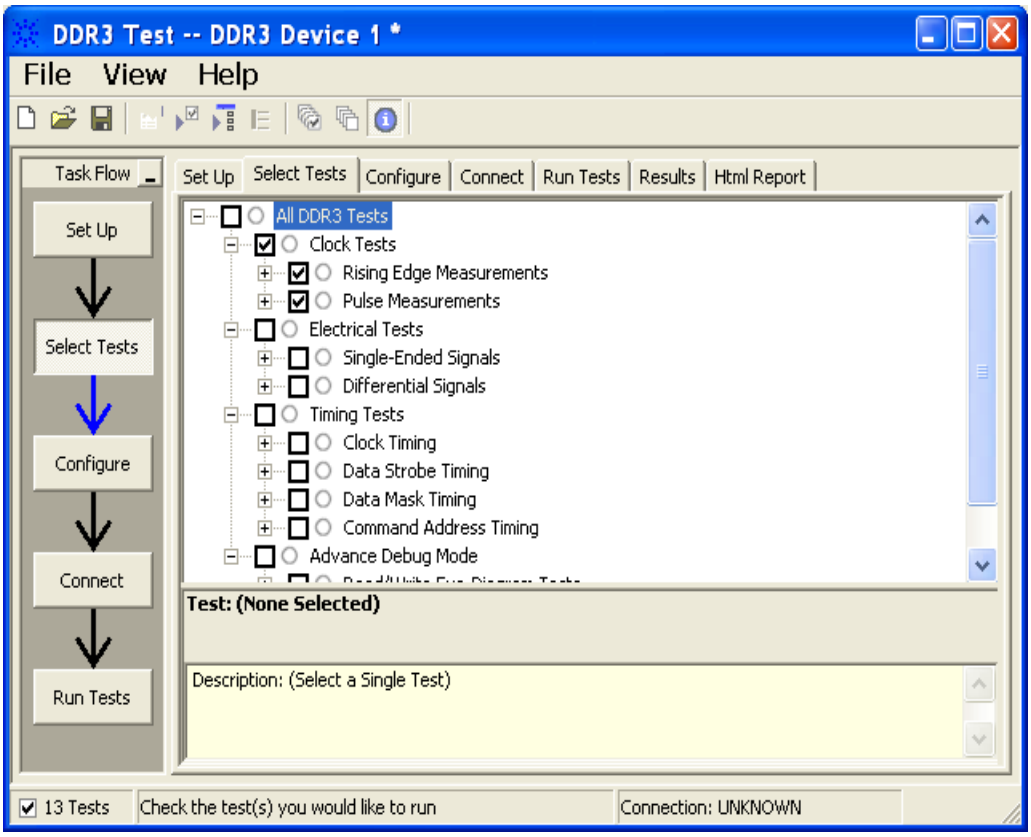


Figure 3 Selecting Measurement Clock Tests

9 Follow the DDR3 Test application's task flow to set up the configuration options (see Table 3), run the test, and view the test results.

Table 3 Test Configuration Options

Configuration Option	Description
Stop on error	Enabling this option will allow error messages to prompt whenever the test criteria is not met. Disabling this option will allow the system to bypass all the error messages that could occur and proceed to the next test. This option is suitable for long hours multiple trials.
Signal Threshold setting by percentage	This option allows you to define the Upper and Lower threshold of the signal by percentage.
VDD	Input supply voltage value.
VDDQ	Input supply voltage for data output.
Vref	Input reference voltage value.
Vih(dc)	Input voltage high value (direct current).
Vih(ac)	Input voltage high value (alternating current).
Vil(dc)	Input voltage low value (direct current).
Vil(ac)	Input voltage low value (alternating current).
Waveform Source	Identifies the source of the data to be analyzed.
Use Recommended Memory Depth	Sets the Memory Depth to the maximum recommended value. Select "No" if you plan to manually select the memory depth.
Use Fixed Sampling Rate and Bandwidth	Sets the Sampling Rate to 20 GSa and Bandwidth to AUTO. Select "No" if you plan to manually select sampling rate or bandwidth settings.
Worst Case Tracking	
Mark Worst Case Cycle	Places markers around the worst case cycles (test-dependent). Slows runtime performance.
terr(nper) SubWindow Range / terr(nper2) SubWindow Range	
terr(nper/nper2) Minimum N Width Value	Sets the lower bound (inclusive) of the inner sliding window for the terr(nper/nper2) series.
terr(nper/nper2) Maximum N Width Value	Sets the upper bound (inclusive) of the inner sliding window for the terr(nper/nper2) series.
Worst Case Definitions	
tCK Rising Edge Test	Select which extreme should be aggregated from trial to trial
tCK(avg) Rising Edge Test	Select which extreme should be aggregated from trial to trial
tjit(per) Rising Edge Test	Select which extreme should be aggregated from trial to trial
terr(2per) Rising Edge Test	Select which extreme should be aggregated from trial to trial

Configuration Option	Description
terr(3per) Rising Edge Test	Select which extreme should be aggregated from trial to trial
terr(4per) Rising Edge Test	Select which extreme should be aggregated from trial to trial
terr(5per) Rising Edge Test	Select which extreme should be aggregated from trial to trial
terr(nper) Rising Edge Test	Select which extreme should be aggregated from trial to trial
terr(nper2) Rising Edge Test	Select which extreme should be aggregated from trial to trial
tCH Average High Pulse Duty Cycle Test	Select which extreme should be aggregated from trial to trial
tCL Average Low Pulse Duty Cycle Test	Select which extreme should be aggregated from trial to trial
tjit(duty-high) Jitter Average High Test	Select which extreme should be aggregated from trial to trial
tjit(duty-low) Jitter Average Low Test	Select which extreme should be aggregated from trial to trial
SR Rising Test	Select which extreme should be aggregated from trial to trial

Clock Period Jitter - tJIT(per) - Test Method of Implementation

This test is applicable to the Rising Edge Measurement. The purpose of this test is to measure the difference between a measured clock period and the average clock period across multiple cycles of the clock. You can specify the rising edge of your signal for this measurement.

Signals of Interest

Based on the test definition (Read cycle only):

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

Test Definition Notes from the Specification

Table 4 Clock Period Jitter Test

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
Clock Period Jitter	tJIT(per)	-100	100	-90	90	ps	

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
Clock Period Jitter	tJIT(per)	-80	80	TBD	TBD	ps	

Pass Condition

The tJIT(per) measurement value should be within the conformance limits as specified in the *JEDEC Standard JESD79-3*.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. This measurement measures the difference between every period inside a 200 cycle window with the average of the whole window.
2. Compare periods with the new average.
3. Check the results for the smallest and largest values (worst case values).

4 Compare the test results against the compliance test limits.

Test References

See Table 66-Timing Parameters by Speed Bin in the *JEDEC Standard JESD79-3*.

Cycle to Cycle Period Jitter - tJIT(cc) - Test Method of Implementation

This test is applicable to the Rising Edge Measurement. The purpose of this test is to measure the difference in the clock period between two consecutive clock cycles. The tJIT(cc) Rising Edge Measurement measures the clock period from the rising edge of a clock cycle to the next rising edge. The test will show a fail status if the total failed waveforms is greater than 0.

Signals of Interest

Based on the test definition:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

Test Definition Notes from the Specification

Table 5 Cycle to Cycle Period Jitter Test

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
Cycle to Cycle Period Jitter	tJIT(cc)	200		180		ps	

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
Cycle to Cycle Period Jitter	tJIT(cc)	160		TBD		ps	

Pass Condition

The tJIT(cc) measurement value should be within the conformance limits as specified in the *JEDEC Standard JESD79-3*.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1 Measure the difference between every adjacent pair of periods.

2 Generate 201 measurement results.

3 Check the results for the smallest and largest values (worst case values).

4 Compare the test results against the compliance test limits.

Test References

See Table 66-Timing Parameters by Speed Bin in the *JEDEC Standard JESD79-3*.

Cumulative Error - tERR(n per) - Test Method of Implementation

This Cumulative Error (across “n” cycles) test is applicable to the Rising Edge Measurement. The purpose of this test is to measure the difference between a measured clock period and the average clock period across multiple cycles of the clock.

Signals of Interest

Based on the test definition:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user’s speed grade selection

Test Definition Notes from the Specification

Table 6 Cumulative Error Across n Cycles

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units
		min	max	min	max	min	max	min	max	
Cumulative error across 2 cycles	tERR(2per)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps
Cumulative error across 3 cycles	tERR(3per)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps
Cumulative error across 4 cycles	tERR(4per)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps
Cumulative error across 5 cycles	tERR(5per)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps
Cumulative error across $6 \le n \le 10$ cycles	tERR(6-10)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps
Cumulative error across $11 \le n \le 50$ cycles	tERR(11-50)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps

Pass Condition

The tERR measurement value should be within the conformance limits as specified in the *JEDEC Standard JESD79-3*.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. tERR(2per) is similar to tJIT(per), except it makes a small 2-cycle window inside the big 200 cycle window and compares the average of the small window with the average of the big window.
2. Check the results for the smallest and largest values (worst case values).
3. Compare the results against the compliance test limits.
4. tERR(3per) is the same as tERR(2per) except the small window size is 3 periods wide. tERR(4per) uses small window size of 4 periods and tERR(5per) uses 5 periods.
5. tERR(6-10per) executes tERR(6per), tERR(7per), tERR(8per), tERR(9per) and tERR(10per), combines all the measurement results together into one big pool and checks for the smallest and largest value.
6. tERR(11-50per) does the same for tERR(11per) through tERR(50per).

Test References

See Table 66-Timing Parameters by Speed Bin in the *JEDEC Standard JESD79-3*.

Average High Pulse Width - tCH(avg) - Test Method of Implementation

The purpose of this test is to measure the average duty cycle of all the positive pulse widths within a window of 200 consecutive cycles.

Signals of Interest

Based on the test definition:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

Test Definition Notes from the Specification

Table 7 Average High Pulse Width Test

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
Average High Pulse Width	tCH(avg)	0.47	0.53	0.47	0.53	tCK(avg)	

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
Average High Pulse Width	tCH(avg)	0.47	0.53	TBD	TBD	tCK(avg)	

Pass Condition

The tCH measurement value should be within the conformance limits as specified in the *JEDEC Standard JESD79-3*.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. Measure the sliding "window" of 200 cycles.
2. Measure the width of the high pulses (1-200, 2-201 and 3-202) and determine the average value for this window.
3. Check the total 3 results for the smallest and largest values (worst case values).
4. Compare the test results against the compliance test limits.

Test References

See Table 66-Timing Parameters by Speed Bin in the *JEDEC Standard JESD79-3*.

Average Low Pulse Width - tCL(avg) - Test Method of Implementation

The purpose of this test is to measure the average duty cycle of all the negative pulse widths within a window of 200 consecutive cycles.

Signals of Interest

Based on the test definition:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

Test Definition Notes from the Specification

Table 8 Average Low Pulse Width Test

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
Average Low Pulse Width	tCL(avg)	0.47	0.53	0.47	0.53	tCK(avg)	

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
Average Low Pulse Width	tCL(avg)	0.47	0.53	TBD	TBD	tCK(avg)	

Pass Condition

The tCL measurement value should be within the conformance limits as specified in the *JEDEC Standard JESD79-3*.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. Measure the sliding "window" of 200 cycles.
2. Measure the width of the low pulses (1-200, 2-201 and 3-202) and determine the average value for this window.
3. Check the total 3 results for the smallest and largest values (worst case values).
4. Compare results against the compliance test limits.

Test References

See Table 66-Timing Parameters by Speed Bin in the *JEDEC Standard JESD79-3*.

Half Period Jitter - tJIT(duty) - Test Method of Implementation

The Half Period Jitter tJIT(duty) can be divided into tJIT(CH) Jitter Average High and tJIT(LH) Jitter Average Low. The tJIT(CH) Jitter Average High Measurement measures between a positive pulse width of a cycle in the waveform, and the average positive pulse width of all cycles in a 200 consecutive cycle window. tJIT(LH) Jitter Average Low Measurement measures between a negative pulse width of a cycle in the waveform and the average negative pulse width of all cycles in a 200 consecutive cycle window.

Signals of Interest

Based on the test definition:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

Test Definition Notes from the Specification

Table 9 Duty Cycle Jitter Test

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
Duty Cycle Jitter	tJIT(duty)	-100	100	-75	75	ps	

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
Duty Cycle Jitter	tJIT(duty)	-60	60	TBD	TBD	ps	

Pass Condition

The tJIT(duty) measurement value should be within the conformance limits as specified in the *JEDEC Standard JESD79-3*.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

tJIT(CH)

1. This measurement measures the difference between every high pulse width inside a 200 cycle window with the average of the whole window.
2. Measure the difference between high pulse width, and the average. Save the answer as the measurement result.
3. Compare the high pulse width with the new average.
4. Check the results for the smallest and largest values (worst case values).
5. Compare the test results against the compliance test limits.

tJIT(LH)

1. This measurement is similar to tJIT(CH) above except, instead of using high pulse widths, it uses low pulse widths for testing comparison.

Test References

See Table 66-Timing Parameters by Speed Bin in the *JEDEC Standard JESD79-3*.

Average Clock Period - tCK(avg) - Test Method of Implementation

This test is applicable to the Rising Edge Measurement. tCK(avg) is average clock period within 200 consecutive cycle window. The tCK(avg) Rising Edge Measurement measures the period from the rising edge of a cycle to the next rising edge within the waveform window.

Signals of Interest

Based on the test definition:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

Test Definition Notes from the Specification

See Table 66-Timing Parameters by Speed Bin in the *JEDEC Standard JESD79-3*.

Pass Condition

The tCK(avg) measurement value should be within the conformance limits as specified in the *JEDEC Standard JESD79-3*.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. This measurement measures a sliding "window" of 200 cycles.
2. Calculate the average period value for periods 1-200, 2-201 and 3-202.
3. Check the results for the smallest and largest values (worst case values).
4. Compare the test results against the compliance test limits.

Test References

See Table 66-Timing Parameters by Speed Bin in the *JEDEC Standard JESD79-3*.

4 Single-Ended Signals AC Input Parameters Tests

This section provides the Methods of Implementation (MOIs) for Single-Ended Signals AC Input tests using an Agilent 54850A series or 80000 series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR3 Compliance Test Application.

Probing for Single-Ended Signals AC Input Parameters Tests

When performing the Single-Ended Signals AC Input Parameters tests, the DDR3 Compliance Test Application will prompt you to make the proper connections. The connection for the Single-Ended Signals AC Input Parameters tests may look similar to the following diagram. Refer to the Connection tab in DDR3 Electrical Performance Compliance application for the exact number of probe connections.

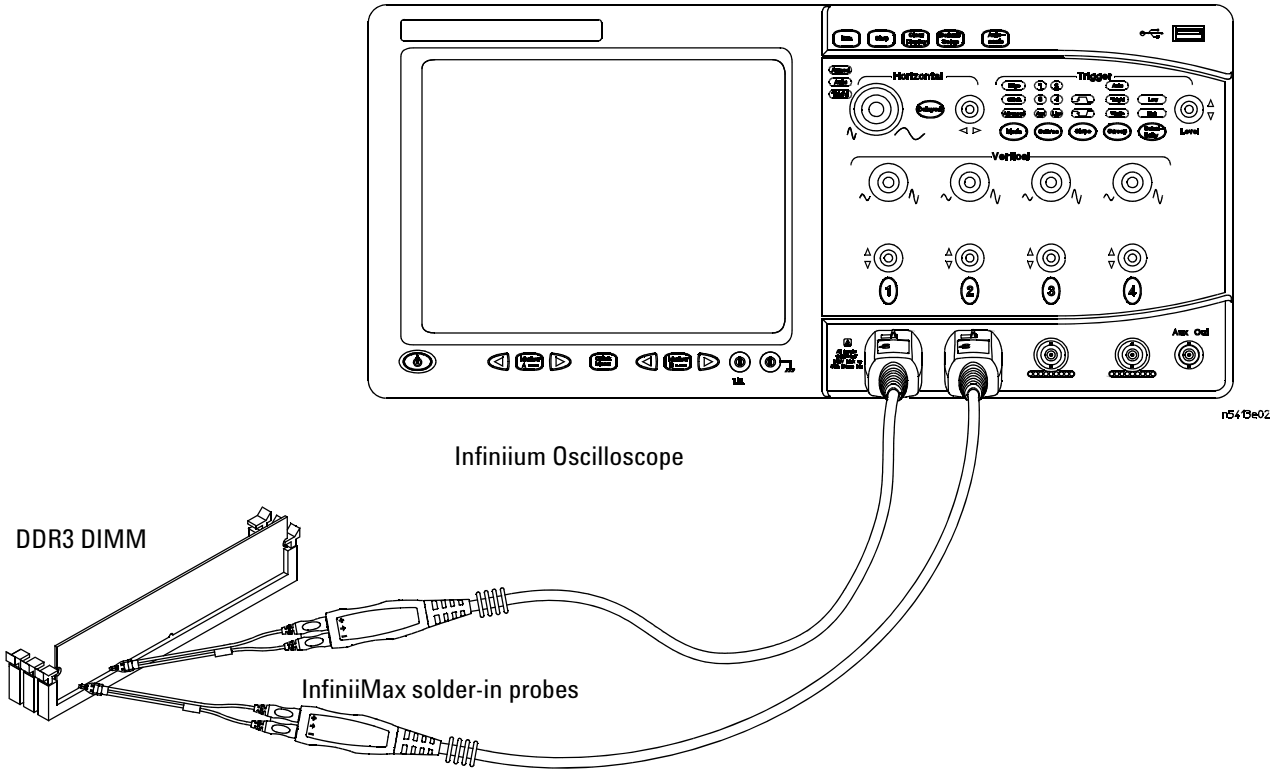


Figure 4 Probing for Single-Ended Signals AC Input Parameters Tests with Two Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR3 Compliance Test Application. (The channels shown in Figure 4 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 16, “InfiniiMax Probing,” starting on page 261.

Test Procedure

1. Start the automated test application as described in “Starting the DDR3 Compliance Test Application" on page 27.
2. Ensure that the RAM reliability test software is running on the computer system where the DDR3 Device Under Test (DUT) is attached. This software will perform a test on all unused RAM on the system by producing a repetitive burst of read-write data signals to the DDR3 memory.
3. Connect the differential solder-in probe head to the PUTs on the DDR3 DIMM.
4. Connect the oscilloscope probes to any channels of the oscilloscope.
5. In the DDR3 Test application, click the Set Up tab.
6. Select the Speed Grade options. For the Single-Ended Signals AC Input Parameters Tests, you can select any speed grade within the selection: DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600.
7. Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.
8. Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

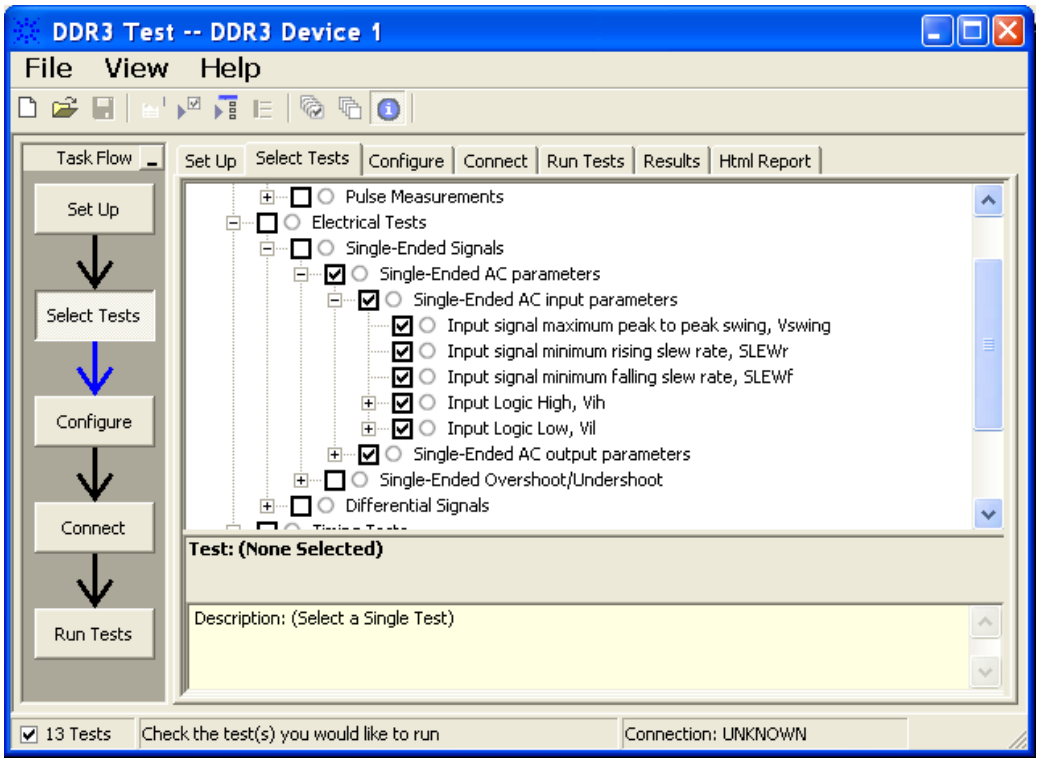


Figure 5 Selecting Single-Ended Signals AC Input Parameters Tests

9 Follow the DDR3 Test application's task flow to set up the configuration options (see Table 10), run the tests and view the tests results.

Table 10 Test Configuration Options

Configuration Option	Description
Stop on error	Enabling this option will allow error messages to prompt whenever the test criteria is not met. Disabling this option will allow the system to bypass all the error messages that could occur and proceed to the next test. This option is suitable for long hours multiple trials.
Signal Threshold setting by percentage	This option allows you to define the Upper and Lower threshold of the signal by percentage.
VDD	Input supply voltage value.
VDDQ	Input supply voltage for data output.
Vref	Input reference voltage value.
Vih(DC)	Input voltage high value (direct current).
Vih(AC)	Input voltage high value (alternating current).
Vil(DC)	Input voltage low value (direct current).
Vil(AC)	Input voltage low value (alternating current).
InfiniiScan Limits	
Read Cycle	
IScan_UL_READ	Identifies the upper limit for Setup Time measurement used in the InfiniiScan Measurement Mode (READ cycle)
IScan_LL_READ	Identifies the lower limit for Setup Time measurement used in the InfiniiScan Measurement Mode (READ cycle)
Write Cycle	
IScan_UL_WRITE	Identifies the upper limit for Setup Time measurement used in the InfiniiScan Measurement Mode (WRITE cycle)
IScan_LL_WRITE	Identifies the lower limit for Setup Time measurement used in the InfiniiScan Measurement Mode (WRITE cycle)
Single-Ended Signals	
Single-Ended AC Parameters	
Pin Under Test, PUT	Identifies the Pin Under Test for Single-Ended AC parameters.
PUT Source	Identifies the source of the PUT to be analyzed for Single-Ended AC tests.
Supporting Pin	Identifies the required supporting pin for Single-Ended AC parameters.
Supporting Pin Source	Identifies the source of the supporting pin for Single-Ended AC Tests.

$V_{SWING(MAX)}$ Test Method of Implementation

$V_{SWING(MAX)}$ - Input Signal Maximum Peak To Peak Swing. The purpose of this test is to verify that the peak-to-peak voltage value of the test signal is lower than the conformance maximum limit of the V_{SWING} value specified in the *JEDEC Standard JESD79-3*.

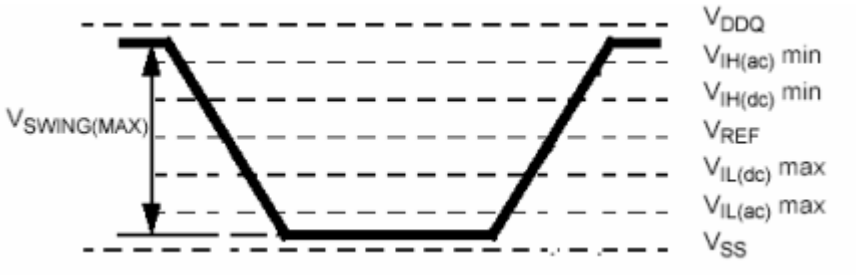


Figure 6 $V_{SWING(MAX)}$

Figure 7 $V_{SWING(MAX)}$ in Infiniium oscilloscope.

Signals of Interest

Based on the test definition (Write cycle only):

- Clock Signal
- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)*
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

Test Definition Notes from the Specification

-

PASS Condition

$\leq V_{SWING(MAX)}$

The peak-to-peak value for the test signal can be lower than or equal to the $V_{SWING(MAX)}$ value.

Measurement Algorithm

1. Calculate the initial time scale value based on the selected DDR3 speed grade options.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Calculate the number of sampling points according to the time scale value.
4. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
5. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.

6 Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.

7 Setup the required scope settings and histogram function settings.

8 Use histogram 'Peak-to-Peak' value as the test result for V_{SWING}.

9 When multiple trials are performed, the largest value (worst case) among the trials will be used as the test result for V_{SWING}.

10 Compare test results against the compliance test limit.

Test References

-

$Slew_R$ Test Method of Implementation

$Slew_R$ - Input Signal Minimum Slew Rate (Rising). The purpose of this test is to verify that the rising slew rate value of the test signal is greater than or equal to the conformance limit of the input SLEW value specified in the *JEDEC Standard JESD79-3*.

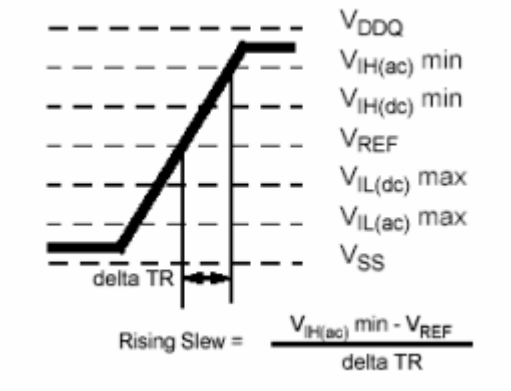


Figure 8 $Slew_R$

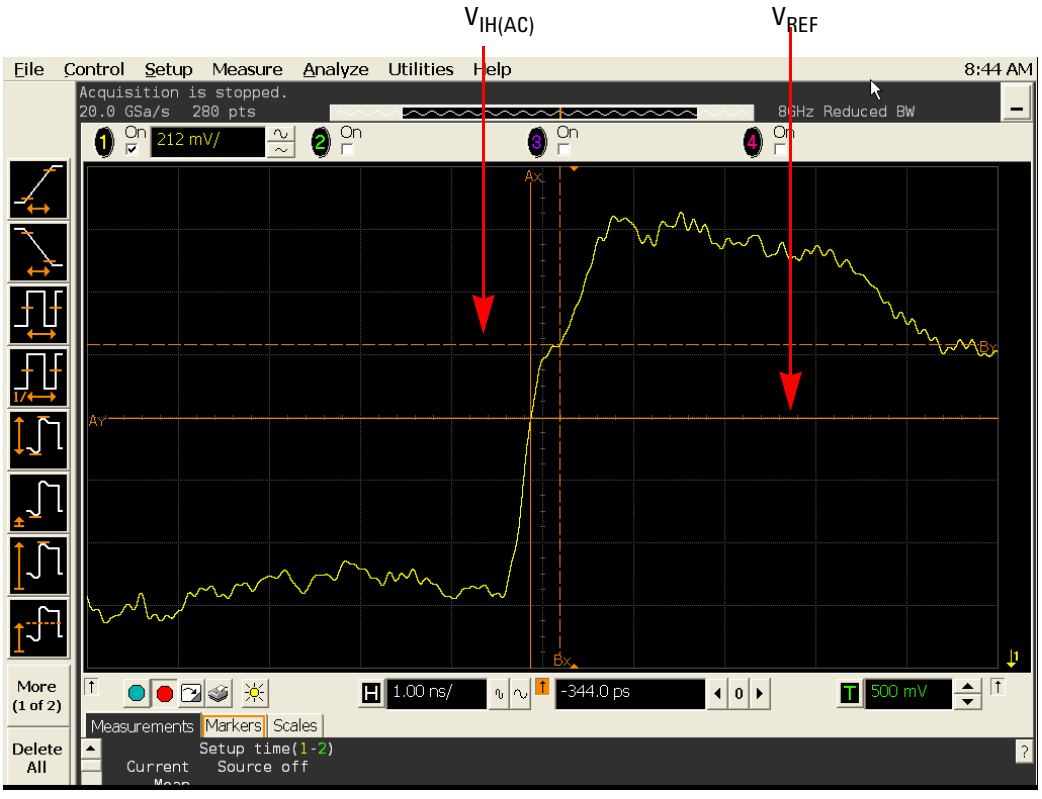


Figure 9 $Slew_R$ in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal
- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)*
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

Test Definition Notes from the Specification

Table 11 Single-ended Input Slew Rate Definition Test

Description	Measured		Defined by	Applicable for
	from	to		
Input slew rate for rising edge	V_{Ref}	$V_{IH(AC)min}$	$\frac{V_{IH(AC)}min - V_{REF}}{\Delta TRS}$	Setup (t_{IS}, t_{DS})
Input slew rate for falling edge	V_{Ref}	$V_{IL(AC)max}$	$\frac{V_{REF} - V_{IL(AC)max}}{\Delta TFS}$	
Input slew rate for rising edge	$V_{IL(DC)max}$	V_{Ref}	$\frac{V_{REF} - V_{IL(DC)max}}{\Delta TFH}$	Hold (t_{IH}, t_{DH})
Input slew rate for falling edge	$V_{IL(DC)min}$	V_{Ref}	$\frac{V_{IH(DC)}min - V_{REF}}{\Delta TRH}$	

PASS Condition

$\geq SLEW_R$

The calculated Rising Slew value for the test signal should be greater than or equal to the SLEW value.

Measurement Algorithm

1. Calculate the initial time scale value based on the selected DDR3 speed grade.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Calculate the number of sampling points according to the time scale value.
4. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
5. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
6. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
7. Setup the required scope settings and histogram function settings.
8. Verify that V_{REF} and $V_{IH(AC)}$ points can be found on the oscilloscope screen.
9. Calculate the delta TR.
10. Calculate Rising Slew.

$$\mathrm{RisingSlew} = \frac{V_{IH(ac)}\mathrm{min} - V_{REF}}{\Delta TR}$$

11. Compare test results against the compliance test limit.

Test References

See Table 29 - Single-ended Input Slew Rate Definition, in the *JEDEC Standard JESD79-3*.

$Slew_F$ Test Method of Implementation

$Slew_F$ - Input Signal Minimum Slew Rate (Falling). The purpose of this test is to verify that the falling slew rate value of the test signal is greater than or equal to the conformance limit of the input SLEW value specified in the *JEDEC Standard JESD79-3*.

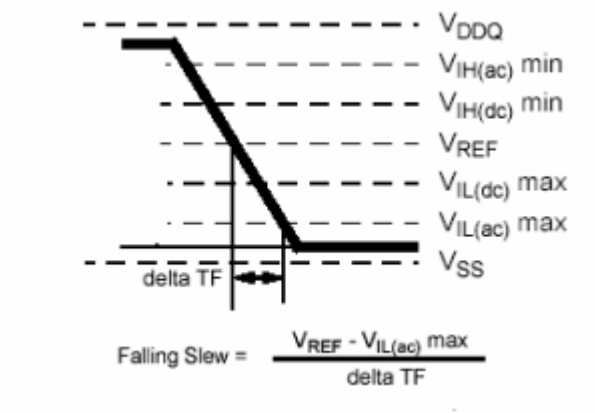


Figure 10 $Slew_F$

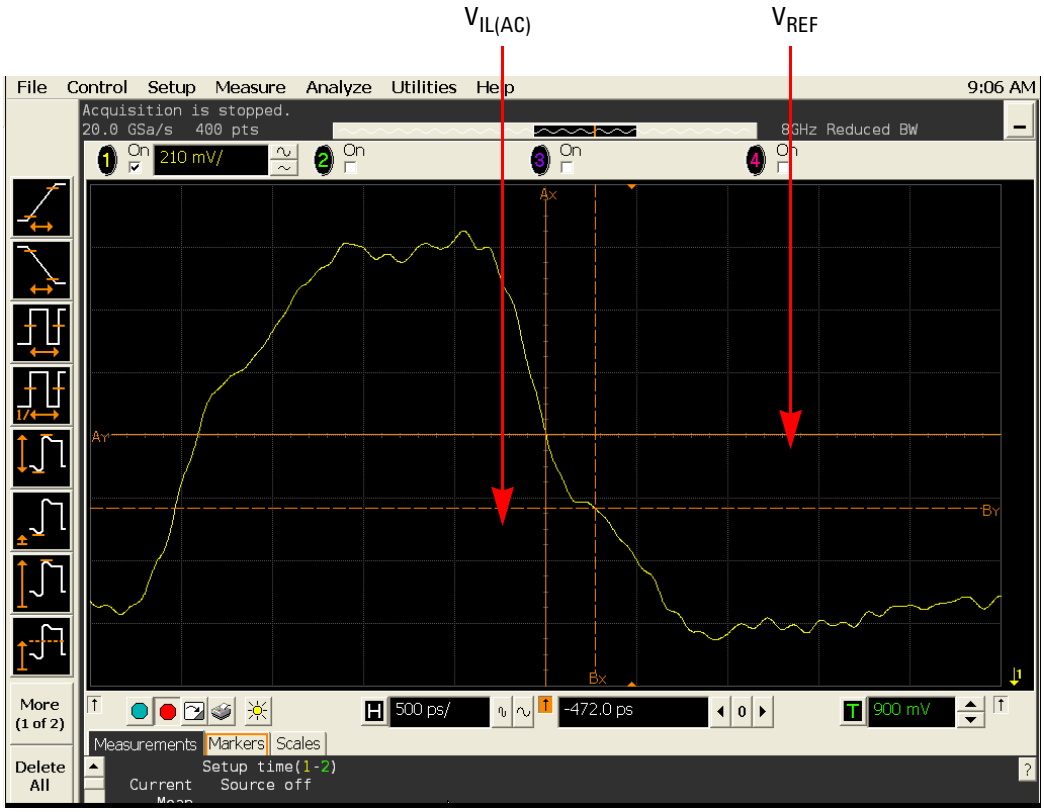


Figure 11 $Slew_F$ in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal
- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)*
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

Test Definition Notes from the Specification

Table 12 Single-ended Input Slew Rate Definition Test

Description	Measured		Defined by	Applicable for
	from	to		
Input slew rate for rising edge	V_{Ref}	$V_{IH(AC)min}$	$\frac{V_{IH(AC)}min - V_{REF}}{\Delta TRS}$	Setup (t_{IS}, t_{DS})
Input slew rate for falling edge	V_{Ref}	$V_{IL(AC)max}$	$\frac{V_{REF} - V_{IL(AC)max}}{\Delta TFS}$	
Input slew rate for rising edge	$V_{IL(DC)max}$	V_{Ref}	$\frac{V_{REF} - V_{IL(DC)max}}{\Delta TFH}$	Hold (t_{IH}, t_{DH})
Input slew rate for falling edge	$V_{IL(DC)min}$	V_{Ref}	$\frac{V_{IH(DC)}min - V_{REF}}{\Delta TRH}$	

PASS Condition

$\geq SLEW_F$

The calculated Rising Slew value for the test signal should be greater than or equal to the SLEW value.

Measurement Algorithm

1. Calculate the initial time scale value based on the selected DDR3 speed grade options.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Calculate the number of sampling points according to the time scale value.
4. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
5. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
6. Perform signal skew checking on DQ-DQS to make sure it can be triggered during Read/Write separation later.
7. Setup the required scope settings and histogram function settings.
8. Verify that V_{REF} and $V_{IL(AC)}$ points can be found on the oscilloscope screen.
9. Calculate the delta TR.
10. Calculate the Falling Slew.

$$\text{FallingSlew} = \frac{V_{REF} - V_{IL(ac)}\text{max}}{\Delta TF}$$

11. Compare test results against the compliance test limit.

Test References

See Table 29 - Single-ended Input Slew Rate Definition, in the *JEDEC Standard JESD79-3*.

$V_{IH(AC)}$ Test Method of Implementation

V_{IH} Input Logic High Test can be divided into two sub tests - $V_{IH(AC)}$ test and $V_{IH(DC)}$ test.

$V_{IH(AC)}$ - Maximum AC Input Logic High. The purpose of this test is to verify that the maximum high level voltage value of the test signal within a valid sampling window is greater than the conformance lower limit of the $V_{IH(AC)}$ value specified in the *JEDEC Standard JESD79-3*.

The value of V_{REF} which directly affects the conformance lower limit is defaulted to 0.9 V. However, users have the flexibility to change this value.

Figure 12 $V_{IH(AC)}$ Test - Maximum AC Input Logic High in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal
- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR

- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)*
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

Test Definition Notes from the Specification

Table 13 Single Ended AC and DC Input Levels

Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600		Units	Notes
		Min	Max		
$V_{IH(AC)}$	AC input logic high	V_{REF} + 0.175	-	V	1, 2

NOTE 1: For DQ and DM, $V_{REF} = V_{REF}DQ$. For input only pins except RESET#, $V_{REF} = V_{REF}CA$.

NOTE 2: Refer to 8.6 Overshoot and Undershoot Specifications at page 113 in the *JEDEC Standard JESD79-3*.

PASS Condition

$\geq V_{IH(ac)}$

The maximum value for the high level voltage should be greater than or equal to the minimum $V_{IH(AC)}$ value.

Measurement Algorithm

1. Calculate the initial time scale value based on the selected DDR3 speed grade options.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Calculate the number of sampling points according to the time scale value.
4. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
5. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.

6 Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.

7 Setup the required scope settings and histogram function settings.

8 Use the histogram **Max** value as the test result for $V_{IH(AC)}$.

9 When multiple trials are performed, the largest value (worst case) among the trials will be used as the test result for $V_{IH(AC)}$.

10 Compare test results against the compliance test limits.

Test References

See Table 26 - Single Ended AC and DC Input Levels, in the *JEDEC Standard JESD79-3*.

$V_{IH(DC)}$ Test Method of Implementation

$V_{IH(DC)}$ - Minimum DC Input Logic High. The purpose of this test is to verify that the minimum high level voltage value of the test signal within a valid sampling window is within the conformance limits of the $V_{IH(DC)}$ value specified in the *JEDEC Standard JESD79-3*.

The value of V_{REF} which directly affects the conformance lower limit is defaulted to 0.9 V. However, users have the flexibility to change this value.

The value of V_{DDQ} which directly affects the conformance upper limit is defaulted to 1.8 V. However, users have the flexibility to change this value as well.

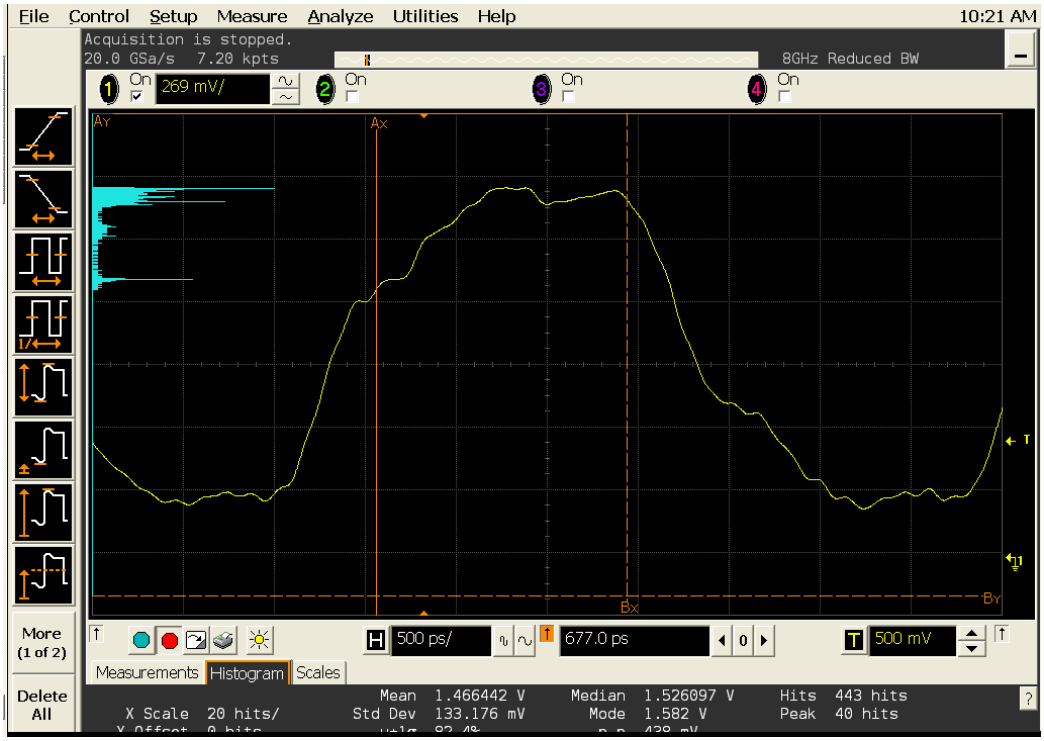


Figure 13 $V_{IH(DC)}$ Test - Minimum DC Input Logic High in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal
- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR

- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)*
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

Test Definition Notes from the Specification

Table 14 Single Ended AC and DC Input Levels

Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600		Units	Notes
		Min	Max		
$V_{IH(DC)}$	DC input logic high	V_{REF} + 0.100	TBD	V	1
$V_{REFDQ(DC)}$	Reference Voltage for DQ, DM inputs	0.49 * VDD	0.51 * VDD	V	3, 4
$V_{REFCA(DC)}$	Reference Voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	V	3, 4

NOTE 1: For DQ and DM, V_{REF} = V_{REF}DQ. For input only pins except RESET#, V_{REF} = V_{REF}CA.

NOTE 3: The AC peak noise on V_{REF} may not allow V_{REF} to deviate from V_{REF}(DC) by more than +/-1% VDD (for reference: approx. +/-15mV)

NOTE 4: For reference: approx. VDD/2 +/-15mV.

PASS Condition

The minimum value for the high level voltage should be greater than or equal to the minimum $V_{IH(DC)}$ value.

The minimum value for the high level voltage should be less than or equal to the maximum $V_{IH(DC)}$ value.

Measurement Algorithm

1. Calculate the initial time scale value based on the selected DDR3 speed grade options.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Calculate the number of sampling points according to the time scale value.

4 Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).

5 Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.

6 Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.

7 Setup the required scope settings and histogram function settings.

8 Use the histogram **Min** value as the test result for $V_{IH(DC)}$.

9 When multiple trials are performed, the largest value (worst case) among the trials will be used as the test result for $V_{IH(DC)}$.

10 Compare test results against the compliance test limits.

Test References

See Table 26 - Single Ended AC and DC Input Levels, in the *JEDEC Standard JESD79-3*.

$V_{IL(AC)}$ Test Method of Implementation

V_{IL} AC Input Logic Low High Test can be divided into two sub tests: $V_{IL(AC)}$ test and $V_{IL(DC)}$ test.

$V_{IL(AC)}$ - Minimum AC Input Logic Low. The purpose of this test is to verify that the minimum low level voltage value of the test signal is lower than the conformance maximum limit of the $V_{IL(AC)}$ value specified in the *JEDEC Standard JESD79-3*.

The value of V_{REF} which directly affects the conformance lower limit is defaulted to 0.9 V. However, users have the flexibility to change this value.

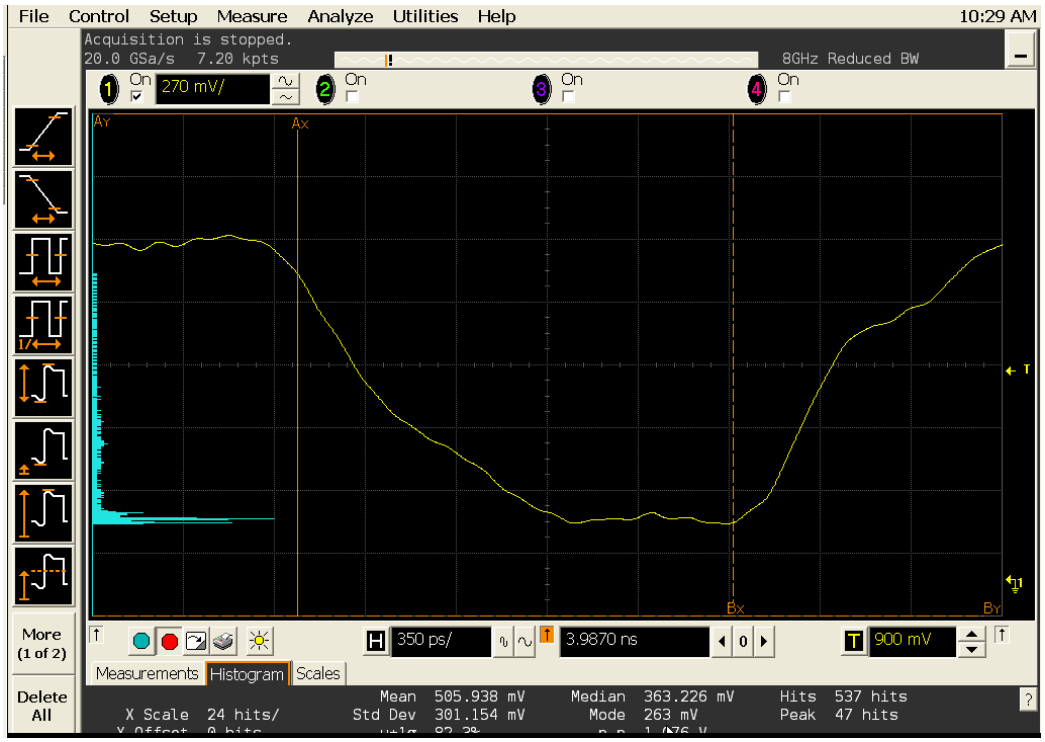


Figure 14 $V_{IL(AC)}$ Test - Minimum AC Input Logic Low in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal
- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR

- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)*
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

Test Definition Notes from the Specification

Table 15 Single Ended AC and DC Input Levels

Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600		Units	Notes
		Min	Max		
$V_{IL(AC)}$	AC input logic low	-	V_{REF} - 0.175	V	1, 2
$V_{REFDQ(DC)}$	Reference Voltage for DQ, DM inputs	0.49 * VDD	0.51 * VDD	V	3, 4
$V_{REFCA(DC)}$	Reference Voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	V	3, 4

NOTE 1: For DQ and DM, V_{REF} = V_{REF}DQ. For input only pins except RESET#, V_{REF} = V_{REF}CA.

NOTE 2: Refer to 8.6 Overshoot and Undershoot Specifications at page 113 in the *JEDEC Standard JESD79-3*.

NOTE 3: The AC peak noise on V_{REF} may not allow V_{REF} to deviate from V_{REF}(DC) by more than +/-1% VDD (for reference: approx. +/-15mV)

NOTE 4: For reference: approx. VDD/2 +/-15mV.

PASS Condition

$\leq V_{IL(AC)}$

The minimum value for the low level voltage should be less than or equal to the maximum $V_{IL(AC)}$ value.

Measurement Algorithm

1. Calculate initial time scale value based on the selected DDR3 speed grade options.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.

3 Calculate the number of sampling points according to the time scale value.

4 Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).

5 Perform signal checking on all the signals in-use in the measurements to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.

6 Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.

7 Setup the required scope settings and histogram function settings.

8 Use the histogram **Min** value as the test result for $V_{IL(AC)}$.

9 When multiple trials are performed, the largest value (worst case) among the trials will be used as the test result for $V_{IL(AC)}$.

10 Compare test results against the compliance test limits.

Test References

See Table 26 - Single Ended AC and DC Input Levels, in the *JEDEC Standard JESD79-3*.

$V_{IL(DC)}$ Test Method of Implementation

$V_{IL(DC)}$ - Maximum DC Input Logic Low. The purpose of this test is to verify that the maximum low level voltage value of the test signal within a valid sampling window is within the conformance limits of the $V_{IL(DC)}$ value specified in the *JEDEC Standard JESD79-3*.

The value of V_{REF} which directly affects the conformance lower limit is defaulted to 0.9 V. However, users have the flexibility to change this value.

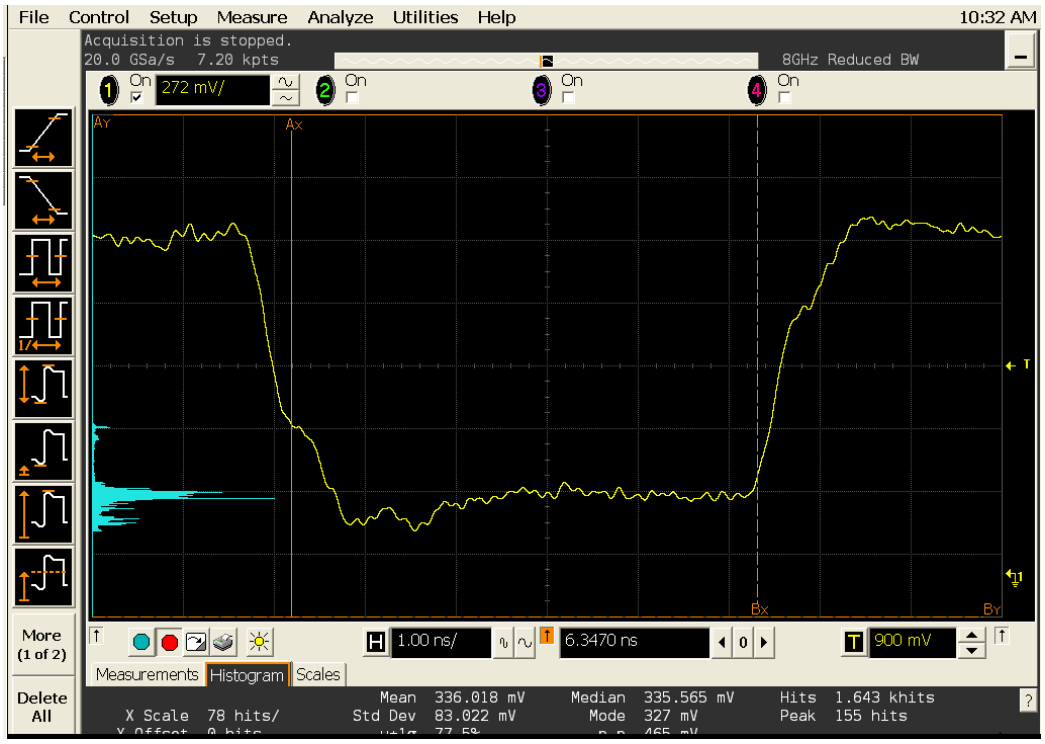


Figure 15 $V_{IL(DC)}$ Test - Maximum DC Input Logic Low in Infiniium oscilloscope.

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal
- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)*
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

Test Definition Notes from the Specification

Table 16 Single Ended AC and DC Input Levels

Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600		Units	Notes
		Min	Max		
$V_{IL(DC)}$	DC input logic low	TBD	V_{REF} - 0.100	V	1
$V_{REFDQ(DC)}$	Reference Voltage for DQ, DM inputs	0.49 * VDD	0.51 * VDD	V	3, 4
$V_{REFCA(DC)}$	Reference Voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	V	3, 4

NOTE 1: For DQ and DM, V_{REF} = V_{REF}DQ. For input only pins except RESET#, V_{REF} = V_{REF}CA.

NOTE 3: The AC peak noise on V_{REF} may not allow V_{REF} to deviate from V_{REF}(DC) by more than +/- 1% VDD (for reference: approx. +/- 15mV)

NOTE 4: For reference: approx. VDD/2 +/- 15mV.

PASS Condition

The maximum value for the low level voltage should be less than or equal to the maximum $V_{IL(DC)}$ value.

The maximum value for the low level voltage should be greater than or equal to the minimum $V_{IL(DC)}$ value.

Measurement Algorithm

1. Calculate the initial time scale value based on the selected DDR3 speed grade options.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Calculate the number of sampling points according to the time scale value.
4. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).

5 Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.

6 Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.

7 Setup the required scope settings and histogram function settings.

8 Use the histogram **Max** value as the test result for $V_{IL(DC)}$.

9 When multiple trials are performed, the largest value (worst case) among all the trials will be used as the test result for $V_{IL(DC)}$.

10 Compare test results against the compliance test limits.

Test References

See Table 26 - Single Ended AC and DC Input Levels, in the *JEDEC Standard JESD79-3*.

5 Single-Ended Signals AC Output Parameters Tests

This section provides the Methods of Implementation (MOIs) for Single-Ended Signals AC Output tests using an Agilent 54850A series or 80000 series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR3 Compliance Test Application.

Probing for Single-Ended Signals AC Output Parameters Tests

When performing the Single-Ended Signals AC Output Parameters tests, the DDR3 Compliance Test Application will prompt you to make the proper connections. The connection for the Single-Ended Signals AC Output Parameters tests may look similar to the following diagram. Refer to the Connection tab in DDR3 Electrical Performance Compliance application for the exact number of probe connections.

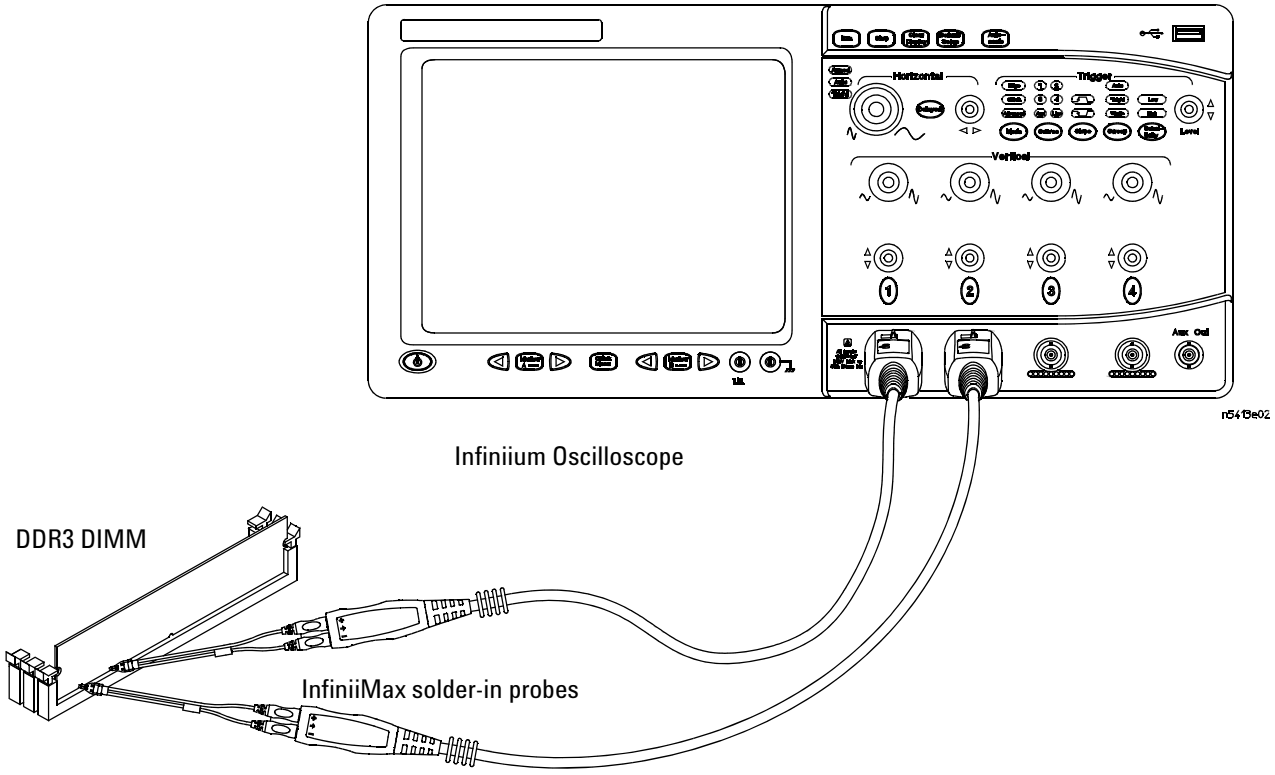


Figure 16 Probing for Single-Ended Signals AC Output Parameters Tests with Two Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR3 Compliance Test Application. (The channels shown in Figure 16 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 16, “InfiniiMax Probing,” starting on page 261.

Test Procedure

1. Start the automated test application as described in “Starting the DDR3 Compliance Test Application" on page 27.
2. Ensure that the RAM reliability test software is running on the computer system where the DDR3 Device Under Test (DUT) is attached. This software will perform a test on all unused RAM on the system by producing a repetitive burst of read-write data signals to the DDR3 memory.
3. Connect the differential solder-in probe head to the PUTs on the DDR3 DIMM.
4. Connect the oscilloscope probes to any channels of the oscilloscope.
5. In the DDR3 Test application, click the Set Up tab.
6. Select the Speed Grade options. For the Single-Ended Signals AC Input Parameters Tests, you can select any speed grade within the selection: DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600.
7. Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.
8. Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

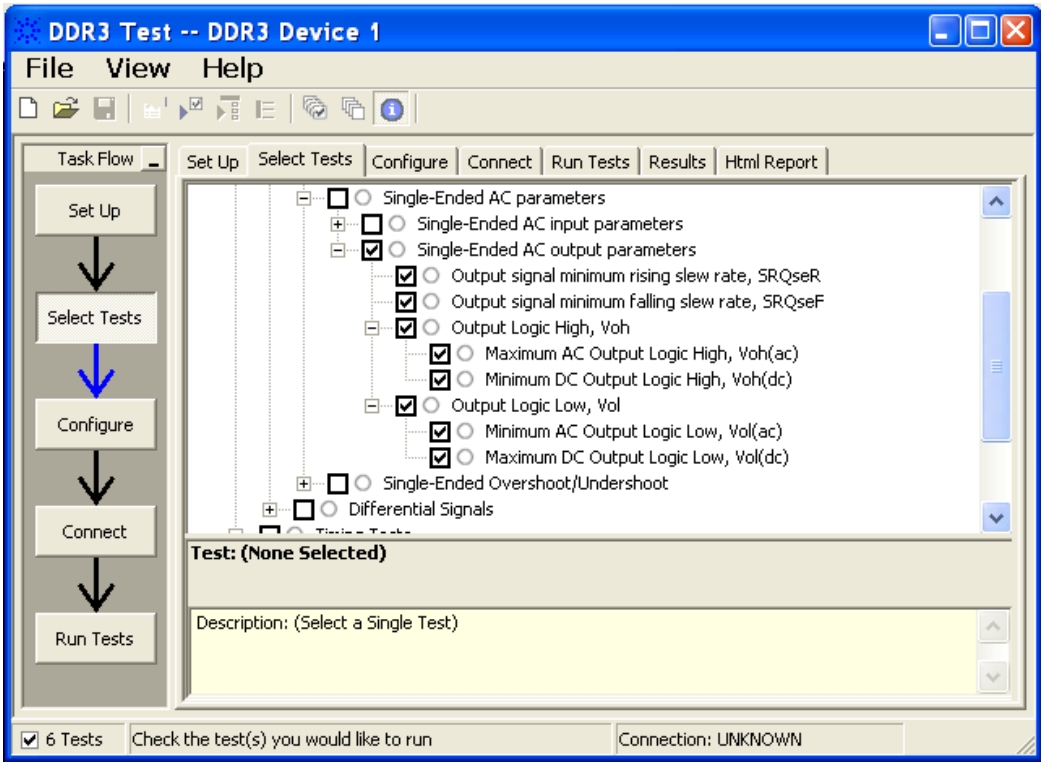


Figure 17 Selecting Single-Ended Signals AC Output Parameters Tests

9 Follow the DDR3 Test application's task flow to set up the configuration options (see Table 17), run the tests and view the tests results.

Table 17 Test Configuration Options

Configuration Option	Description
Stop on error	Enabling this option will allow error messages to prompt whenever the test criteria is not met. Disabling this option will allow the system to bypass all the error messages that could occur and proceed to the next test. This option is suitable for long hours multiple trials.
Signal Threshold setting by percentage	This option allows you to define the Upper and Lower threshold of the signal by percentage.
VDD	Input supply voltage value.
VDDQ	Input supply voltage for data output.
Vref	Input reference voltage value.
Vih(DC)	Input voltage high value (direct current).
Vih(AC)	Input voltage high value (alternating current).
Vil(DC)	Input voltage low value (direct current).
Vil(AC)	Input voltage low value (alternating current).
InfiniiScan Limits	
Read Cycle	
IScan_UL_READ	Identifies the upper limit for Setup Time measurement used in the InfiniiScan Measurement Mode (READ cycle)
IScan_LL_READ	Identifies the lower limit for Setup Time measurement used in the InfiniiScan Measurement Mode (READ cycle)
Write Cycle	
IScan_UL_WRITE	Identifies the upper limit for Setup Time measurement used in the InfiniiScan Measurement Mode (WRITE cycle)
IScan_LL_WRITE	Identifies the lower limit for Setup Time measurement used in the InfiniiScan Measurement Mode (WRITE cycle)
Single-Ended Signals	
Single-Ended AC Parameters	
Pin Under Test, PUT	Identifies the Pin Under Test for Single-Ended AC parameters.
PUT Source	Identifies the source of the PUT to be analyzed for Single-Ended AC tests.
Supporting Pin	Identifies the required supporting pin for Single-Ended AC parameters.
Supporting Pin Source	Identifies the source of the supporting pin for Single-Ended AC Tests.

SRQseR Test Method of Implementation

SRQseR - Output Signal Minimum Rising Slew Rate (Rising). The purpose of this test is to verify that the rising slew rate value of the test signal is greater than or equal to the conformance limit of the output SLEW value specified in the *JEDEC Standard JESD79-3*.

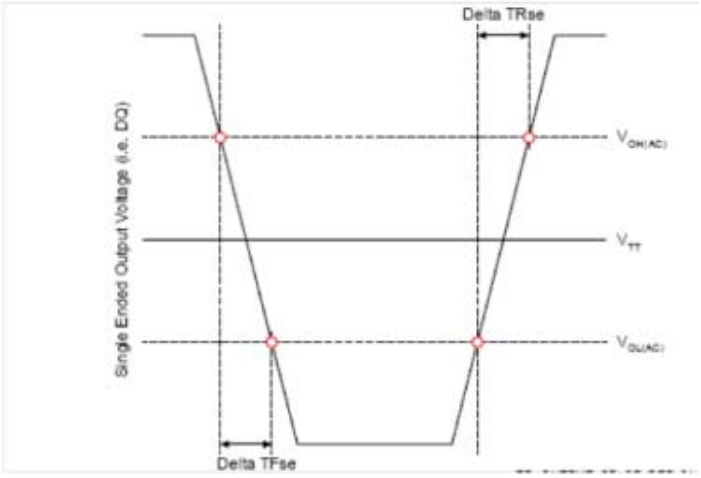


Figure 18 SRQseR

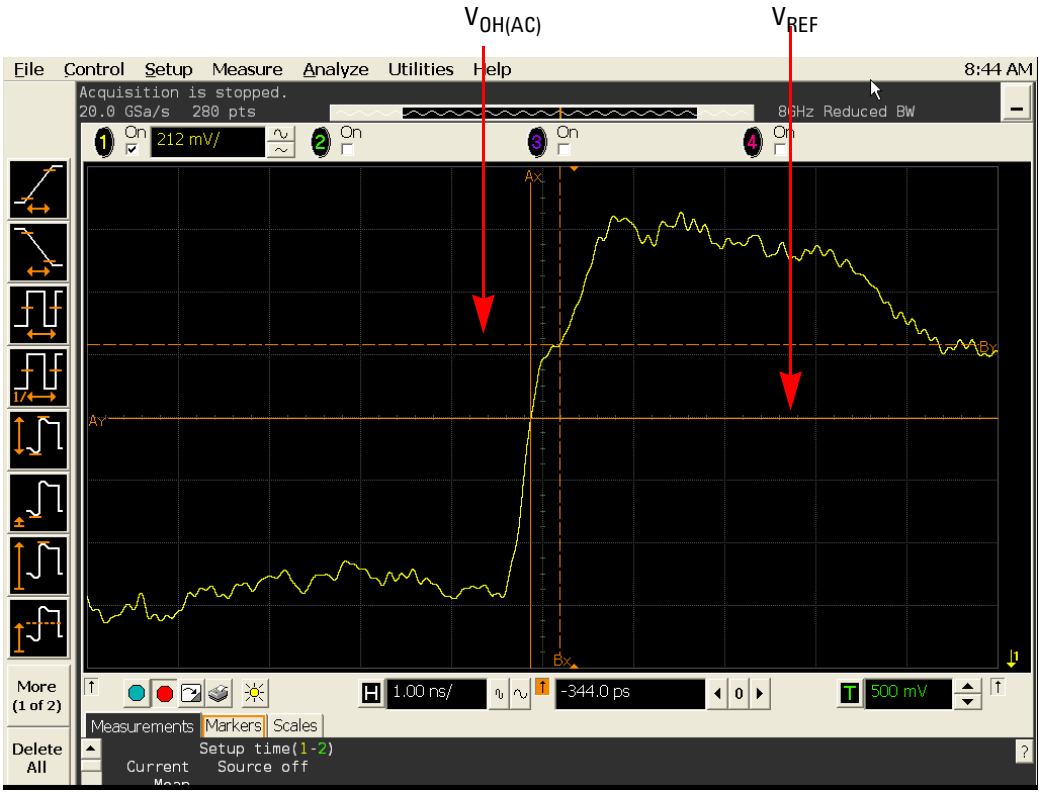


Figure 19 SRQseR in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Read cycle only):

- Data Signal
- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)*
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

Test Definition Notes from the Specification

Table 18 Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$\frac{V_{OH(AC)}-V_{OL(AC)}}{\Delta TRse}$
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$\frac{V_{OH(AC)}-V_{OL(AC)}}{\Delta TFse}$

Table 19 Output Slew Rate (Single-Ended)

Parameters	Symbol	DDR3-800		DDR3-1066		DDR3-1333,		DDR3-1600		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Single-ended Output Slew Rate	SRQse	2.5	5	2.5	5	2.5	5	TBD	5	V/ns

PASS Condition

The calculated Rising Slew value for the test signal should be greater than or equal to the SLEW value.

Measurement Algorithm

1. Calculate the initial time scale value based on the selected DDR3 speed grade.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Calculate the number of sampling points according to the time scale value.
4. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
5. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
6. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
7. Setup the required scope settings and histogram function settings.
8. Verify that V_{REF} and $V_{OH(AC)}$ points can be found on the oscilloscope screen.

9 Calculate the delta TR.

10 Calculate the Rising Slew.

11 When multiple trials are performed, the smallest value (worst case) among all the trials will be used as the test result for SRQseR.

12 Compare test results against the compliance test limit.

Test References

See Table 33 - Single-ended Output Slew Rate Definition and Table 34 - Output Slew Rate (Single-ended), in the *JEDEC Standard JESD79-3*.

SRQseF Test Method of Implementation

SRQseF - Output Signal Minimum Rising Slew Rate (Falling). The purpose of this test is to verify that the falling slew rate value of the test signal is greater than or equal to the conformance limit of the output SLEW value specified in the *JEDEC Standard JESD79-3*.

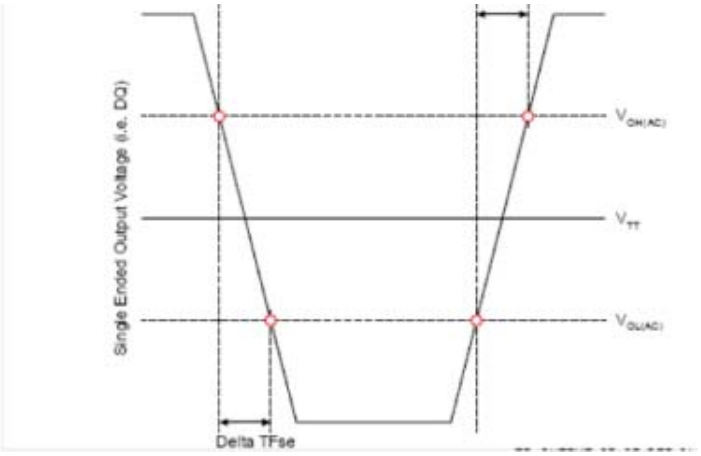


Figure 20 SRQseF

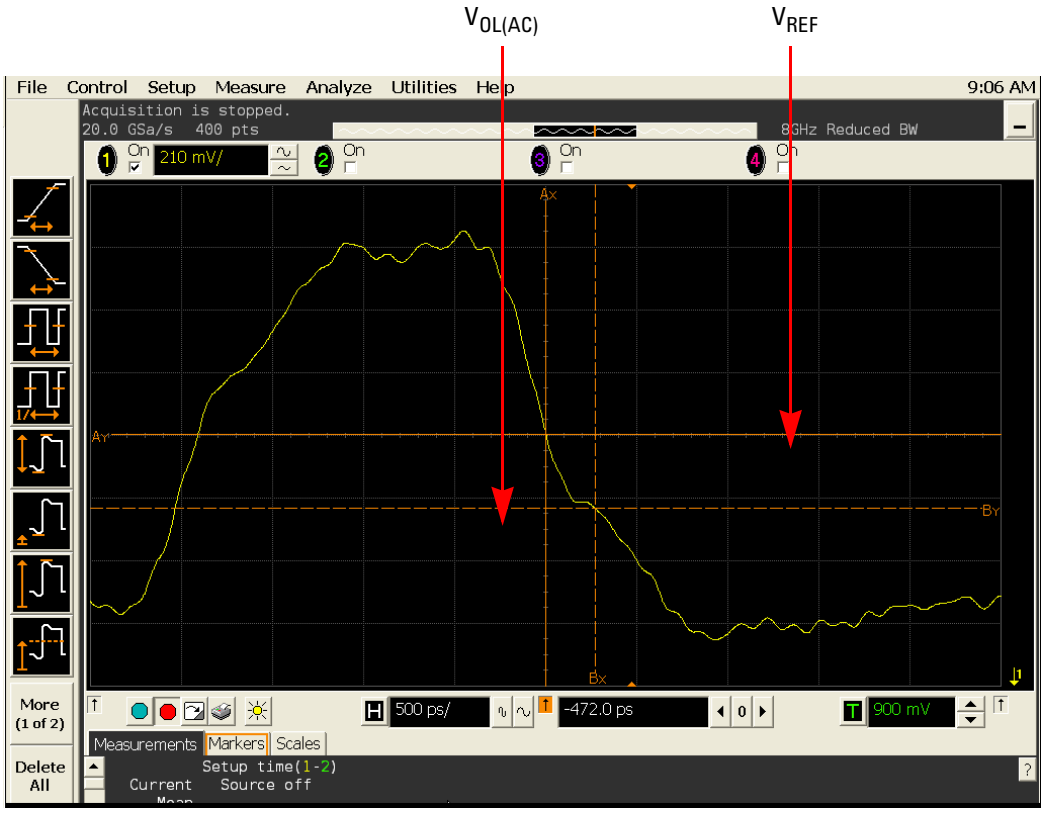


Figure 21 SRQseF in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Read cycle only):

- Data Signal
- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)*
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

Test Definition Notes from the Specification

Table 20 Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$\frac{V_{OH(AC)}-V_{OL(AC)}}{\Delta TRse}$
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$\frac{V_{OH(AC)}-V_{OL(AC)}}{\Delta TFse}$

Table 21 Output Slew Rate (Single-Ended)

Parameters	Symbol	DDR3-800		DDR3-1066		DDR3-1333,		DDR3-1600		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Single-ended Output Slew Rate	SRQse	2.5	5	2.5	5	2.5	5	TBD	5	V/ns

PASS Condition

The calculated Rising Slew value for the test signal should be greater than or equal to the SLEW value.

Measurement Algorithm

1. Calculate the initial time scale value based on the selected DDR3 speed grade options.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Calculate the number of sampling points according to the time scale value.
4. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
5. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
6. Perform signal skew checking on DQ-DQS to make sure it can be triggered during Read/Write separation later.
7. Setup the required scope settings and histogram function settings.
8. Verify that V_{REF} and $V_{IL(AC)}$ points can be found on the oscilloscope screen.

9 Calculate the delta TR.

10 Calculate the Falling Slew.

11 When multiple trials are performed, the smallest value (worst case) among all the trials will be used as the test result for SRQseF.

12 Compare test results against the compliance test limit.

Test References

See Table 33 - Single-ended Output Slew Rate Definition and Table 34 - Output Slew Rate (Single-ended), in the *JEDEC Standard JESD79-3*.

$V_{OH(AC)}$ Test Method of Implementation

V_{OH} Output Logic High Test can be divided into two sub tests - $V_{OH(AC)}$ test and $V_{OH(DC)}$ test.

$V_{OH(AC)}$ - Maximum AC Output Logic High. The purpose of this test is to verify that the maximum high level voltage value of the test signal within a valid sampling window is greater than the conformance lower limit of the $V_{OH(AC)}$ value specified in the *JEDEC Standard JESD79-3*.

The value of V_{REF} which directly affects the conformance lower limit is defaulted to 0.9 V. However, users have the flexibility to change this value.

Figure 22 $V_{OH(AC)}$ Test - Maximum AC Output Logic High in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Read cycle only):

- Data Signal
- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR

- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)*
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

Test Definition Notes from the Specification

Table 22 Single Ended AC and DC Output Levels

Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600	Units	Notes
$V_{OH(AC)}$	AC output logic high measurement level (for output SR)	V_{TT} + 0.1 X V_{DDQ}	V	1

NOTE 1: The swing of ±0.1 x V_{DDQ} is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to V_{TT} = V_{DDQ}/2.

PASS Condition

The maximum value for the high level voltage should be greater than or equal to the minimum $V_{OH(AC)}$ value.

Measurement Algorithm

1. Calculate the initial time scale value based on the selected DDR3 speed grade options.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Calculate the number of sampling points according to the time scale value.
4. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
5. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
6. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
7. Setup the required scope settings and histogram function settings.

8 Use the histogram **Max** value as the test result for $V_{OH(AC)}$.

9 When multiple trials are performed, the largest value (worst case) among the trials will be used as the test result for $V_{OH(AC)}$.

10 Compare test results against the compliance test limits.

Test References

See Table 31 - Single Ended AC and DC Output Levels, in the *JEDEC Standard JESD79-3*.

$V_{OH(DC)}$ Test Method of Implementation

$V_{OH(DC)}$ - Minimum DC Output Logic High. The purpose of this test is to verify that the minimum high level voltage value of the test signal within a valid sampling window is within the conformance limits of the $V_{OH(DC)}$ value specified in the *JEDEC Standard JESD79-3*.

The value of V_{REF} which directly affects the conformance lower limit is defaulted to 0.9 V. However, users have the flexibility to change this value.

The value of V_{DDQ} which directly affects the conformance upper limit is defaulted to 1.8 V. However, users have the flexibility to change this value as well.

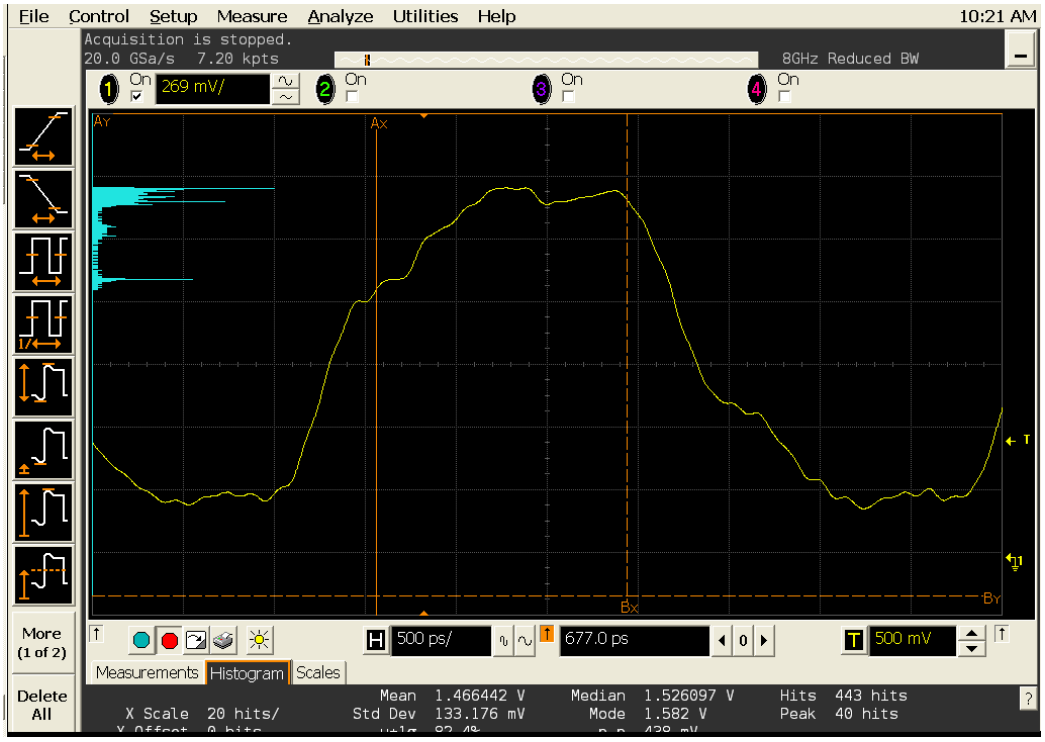


Figure 23 $V_{OH(DC)}$ Test - Minimum DC Output Logic High in Infiniium oscilloscope.

Signals of Interest

Based on the test definition (Read cycle only):

- Data Signal
- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR

- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)*
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

Test Definition Notes from the Specification

Table 23 Single Ended AC and DC Output Levels

Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600	Units
$V_{OH(DC)}$	DC output logic high measurement level (for IV curve linearity)	0.8 X V_{DDQ}	V

PASS Condition

The minimum value for the high level voltage should be greater than or equal to the minimum $V_{OH(DC)}$ value.

The minimum value for the high level voltage should be less than or equal to the maximum $V_{OH(DC)}$ value.

Measurement Algorithm

1. Calculate the initial time scale value based on the selected DDR3 speed grade options.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Calculate the number of sampling points according to the time scale value.
4. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
5. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
6. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
7. Setup the required scope settings and histogram function settings.
8. Use the histogram **Min** value as the test result for $V_{OH(DC)}$.

9 When multiple trials are performed, the largest value (worst case) among the trials will be used as the test result for $V_{OH(DC)}$.

10 Compare test results against the compliance test limits.

Test References

See Table 31 - Single-ended AC and DC Output Levels, in the *JEDEC Standard JESD79-3*.

$V_{OL(AC)}$ Test Method of Implementation

V_{OL} AC Output Logic Low High Test can be divided into two sub tests: $V_{OL(AC)}$ test and $V_{OL(DC)}$ test.

$V_{OL(AC)}$ - Minimum AC Output Logic Low. The purpose of this test is to verify that the minimum low level voltage value of the test signal is lower than the conformance maximum limit of the $V_{OL(AC)}$ value specified in the *JEDEC Standard JESD79-3*.

The value of V_{REF} which directly affects the conformance lower limit is defaulted to 0.9 V. However, users have the flexibility to change this value.

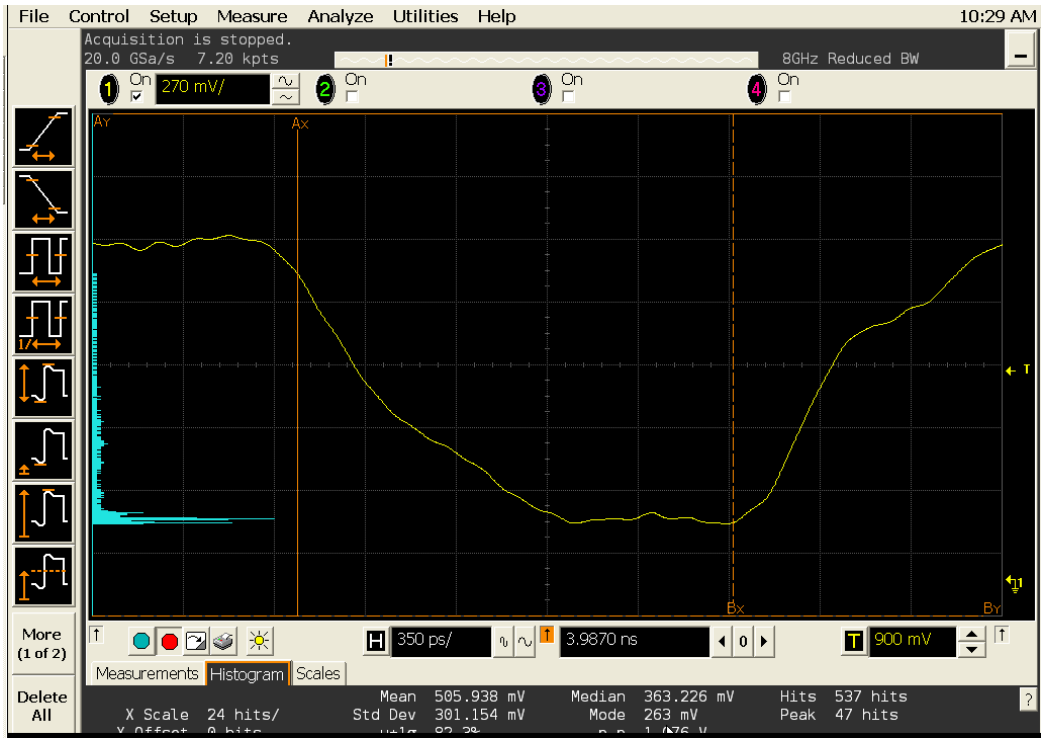


Figure 24 $V_{OL(AC)}$ Test - Minimum AC Output Logic Low in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Read cycle only):

- Data Signal
- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR

- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)*
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

Test Definition Notes from the Specification

Table 24 Single Ended AC and DC Output Levels

Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600	Units	Notes
$V_{OL(AC)}$	AC output low measurement level (for output SR)	V_{TT} - 0.1 X V_{DDQ}	V	1

NOTE 1: The swing of ±0.1 x V_{DDQ} is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to V_{TT} = V_{DDQ}/2.

PASS Condition

The minimum value for the low level voltage should be less than or equal to the maximum $V_{OL(AC)}$ value.

Measurement Algorithm

1. Calculate initial time scale value based on the selected DDR3 speed grade options.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Calculate the number of sampling points according to the time scale value.
4. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
5. Perform signal checking on all the signals in-use in the measurements to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
6. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
7. Setup the required scope settings and histogram function settings.

8 Use the histogram **Min** value as the test result for $V_{OL(AC)}$.

9 When multiple trials are performed, the largest value (worst case) among the trials will be used as the test result for $V_{OL(AC)}$.

10 Compare test results against the compliance test limits.

Test References

See Table 31 - Single-ended AC and DC Output Levels, in the *JEDEC Standard JESD79-3*.

$V_{OL(DC)}$ Test Method of Implementation

$V_{OL(DC)}$ - Maximum DC Output Logic Low. The purpose of this test is to verify that the maximum low level voltage value of the test signal within a valid sampling window is within the conformance limits of the $V_{OL(DC)}$ value specified in the *JEDEC Standard JESD79-3*.

The value of V_{REF} which directly affects the conformance lower limit is defaulted to 0.9 V. However, users have the flexibility to change this value.

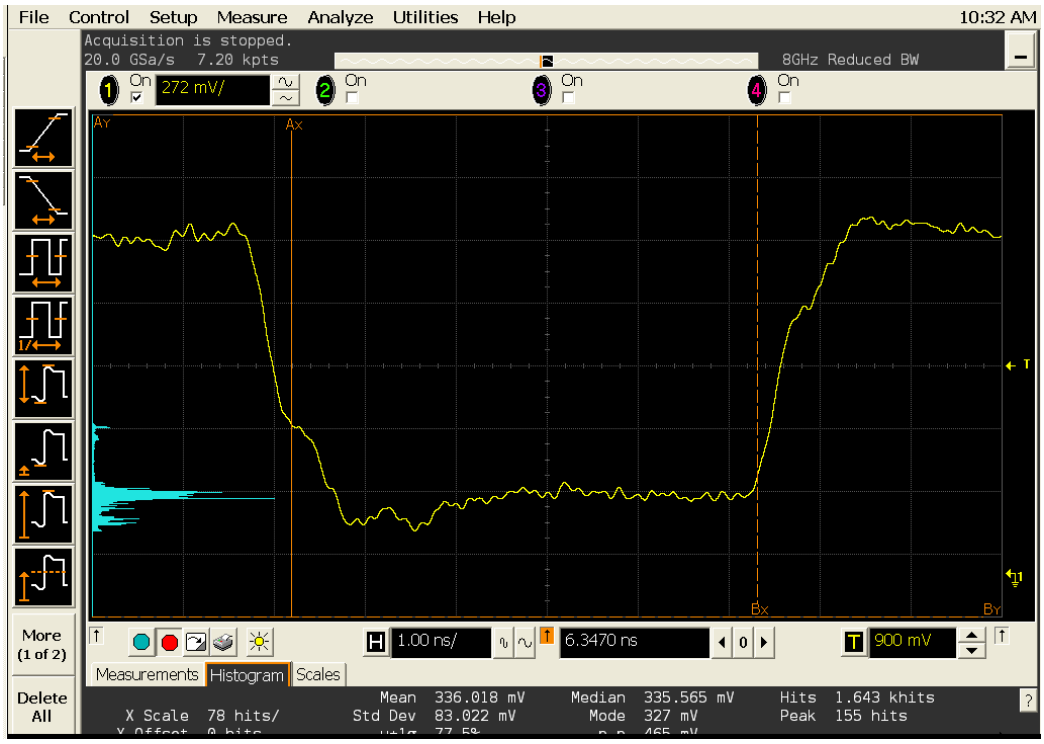


Figure 25 $V_{OL(DC)}$ Test - Maximum DC Output Logic Low in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Read cycle only):

- Data Signal
- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)*
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

Test Definition Notes from the Specification

Table 25 Single Ended AC and DC Output Levels

Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600	Units
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	0.2 X V_{DDQ}	V

PASS Condition

The maximum value for the low level voltage should be less than or equal to the maximum $V_{OL(DC)}$ value.

The maximum value for the low level voltage should be greater than or equal to the minimum $V_{OL(DC)}$ value.

Measurement Algorithm

1. Calculate the initial time scale value based on the selected DDR3 speed grade options.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Calculate the number of sampling points according to the time scale value.
4. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
5. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
6. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
7. Setup the required scope settings and histogram function settings.
8. Use the histogram **Max** value as the test result for $V_{OL(DC)}$.
9. When multiple trials are performed, the largest value (worst case) among all the trials will be used as the test result for $V_{OL(DC)}$.

10 Compare test results against the compliance test limits.

Test References

See Table 31 - Single-ended AC and DC Output Levels, in the *JEDEC Standard JESD79-3*.

6 Single-Ended Signals Overshoot/Undershoot Tests

This section provides the Methods of Implementation (MOIs) for Single-Ended Signals Overshoot/Undershoot tests using an Agilent 54850A series or 80000 series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR3 Compliance Test Application.

Probing for Overshoot/Undershoot Tests

When performing the Single-Ended Signals Overshoot/Undershoot tests, the DDR3 Compliance Test Application will prompt you to make the proper connections as shown in the following diagram. Refer to the Connection tab in DDR3 Electrical Performance Compliance application for the exact number of probe connections.

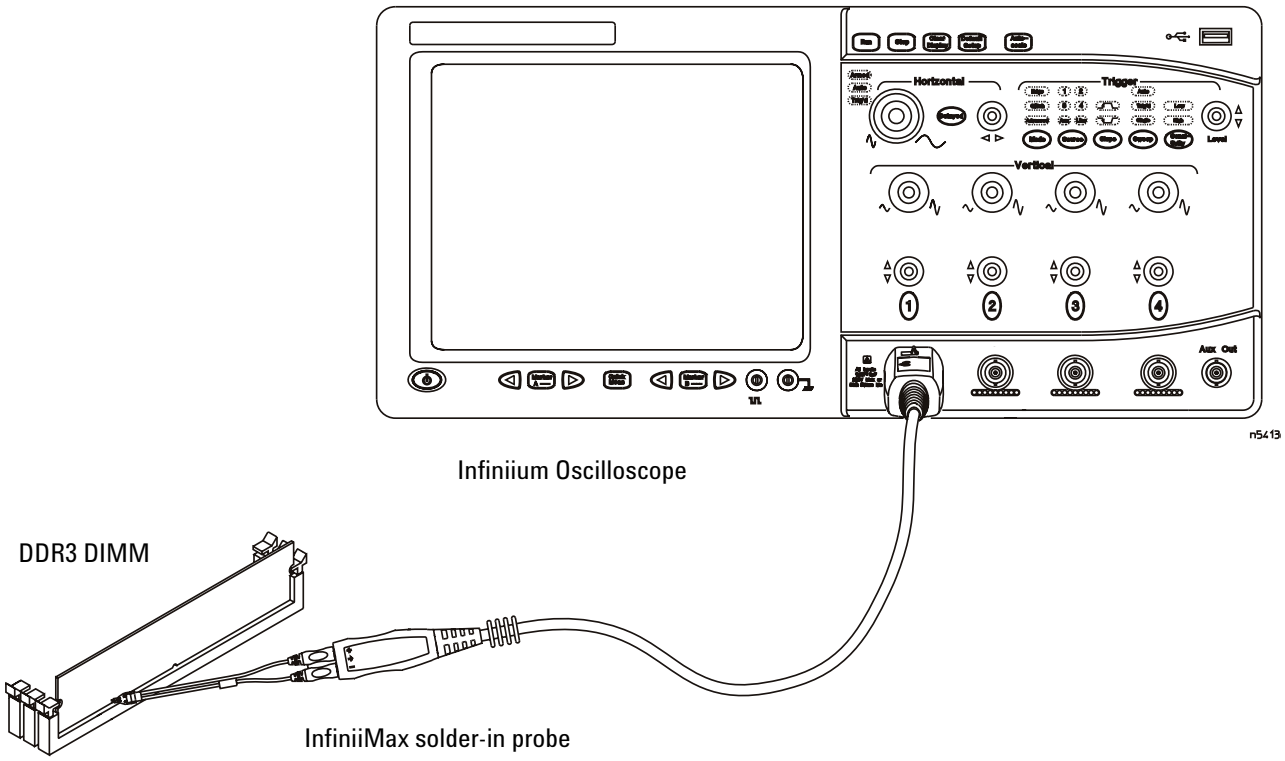


Figure 26 Probing for Single-Ended Signals Overshoot/Undershoot Tests

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR3 Compliance Test Application. (The channel shown in Figure 26 is just an example).

For more information on the probe amplifiers and differential probe heads, see Chapter 16, “InfiniiMax Probing,” starting on page 261.

Test Procedure

1. Start the automated test application as described in “Starting the DDR3 Compliance Test Application" on page 27.
2. Ensure that the RAM reliability test software is running on the computer system where the DDR3 Device Under Test (DUT) is attached. This software will perform test on all unused RAM on the system by producing repetitive burst of read-write data signals to the DDR3 memory.
3. Connect the differential solder-in probe head to the PUTs on the DDR3 DIMM.
4. Connect the oscilloscope probes to any channels of the oscilloscope.
5. In the DDR3 Test application, click the Set Up tab.
6. Select the Speed Grade options. For Single-Ended Signals Overshoot/Undershoot tests, you can select any speed grade within the selection: DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600.
7. Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.
8. Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

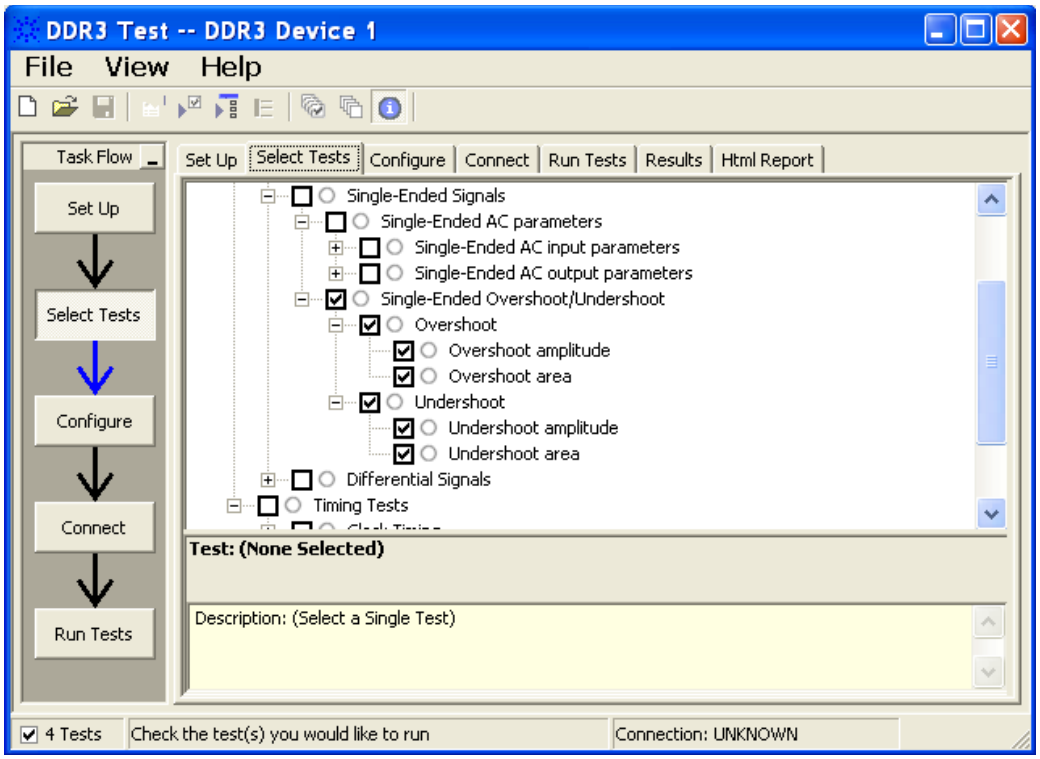


Figure 27 Selecting Single-Ended Signals Overshoot/Undershoot Tests

9 Follow the DDR3 Test application's task flow to set up the configuration options (see Table 26), run the tests and view the tests results.

Table 26 Test Configuration Options

Configuration Option	Description
Stop on error	Enabling this option will allow error messages to prompt whenever the test criteria is not met. Disabling this option will allow the system to bypass all the error messages that could occur and proceed to the next test. This option is suitable for long hours multiple trials.
Signal Threshold setting by percentage	This option allows you to define the Upper and Lower threshold of the signal by percentage.
VDD	Input supply voltage value.
VDDQ	Input supply voltage for data output.
Vref	Input reference voltage value.
Vih(DC)	Input voltage high value (direct current).
Vih(AC)	Input voltage high value (alternating current).
Vil(DC)	Input voltage low value (direct current).
Vil(AC)	Input voltage low value (alternating current).
InfiniiScan Limits	
Read Cycle	
IScan_UL_READ	Identifies the upper limit for Setup Time measurement used in the InfiniiScan Measurement Mode (READ cycle)
IScan_LL_READ	Identifies the lower limit for Setup Time measurement used in the InfiniiScan Measurement Mode (READ cycle)
Write Cycle	
IScan_UL_WRITE	Identifies the upper limit for Setup Time measurement used in the InfiniiScan Measurement Mode (WRITE cycle)
IScan_LL_WRITE	Identifies the lower limit for Setup Time measurement used in the InfiniiScan Measurement Mode (WRITE cycle)
Single-Ended Signals	
Single-Ended Overshoot/Undershoot	
Pin Under Test, PUT	Identifies the Pin Under Test for Single-Ended Overshoot/Undershoot.
PUT Source	Identifies the source of the PUT to be analyzed for Single-Ended AC tests.

AC Overshoot Test Method of Implementation

The Overshoot test can be divided into two sub-tests: Overshoot amplitude and Overshoot area. The purpose of this test is to verify that the overshoot value of the test signal is lower than or equal to the conformance limit of the maximum peak amplitude allowed for overshoot as specified in the *JEDEC Standard JESD79-3*.

When there is an overshoot, the area is calculated based on the overshoot width. The Overshoot area should be lower than or equal to the conformance limit of the maximum Overshoot area allowed as specified in the *JEDEC Standard JESD79-3*.

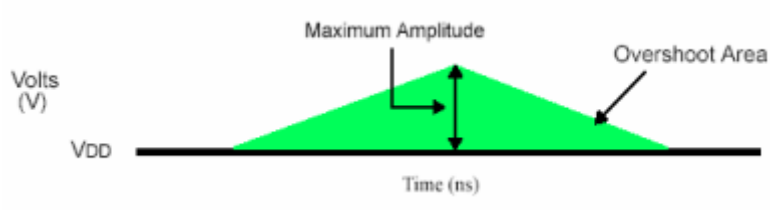


Figure 28 AC Overshoot

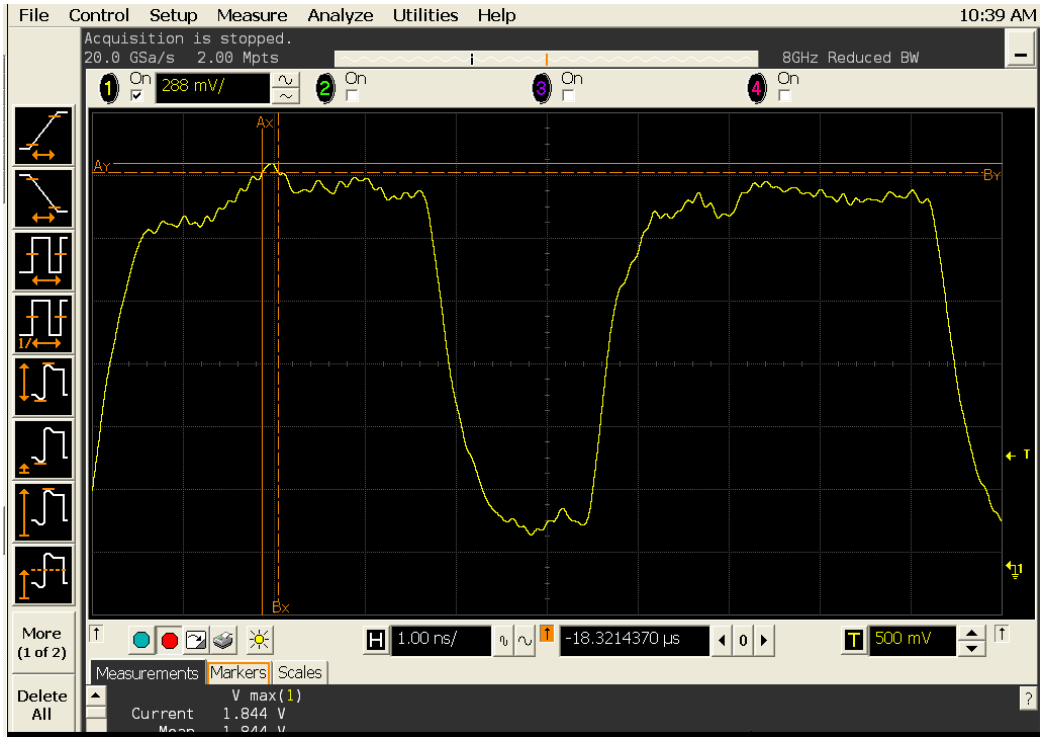


Figure 29 AC Overshoot in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal
- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)*
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

Test Definition Notes from the Specification

Table 27 AC Overshoot/Undershoot Specification for Address and Control Pins

A0-A15, BA0-BA3, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE, ODT

Parameter	Specification			
	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600
Maximum peak amplitude allowed for overshoot area	0.4 V	0.4 V	0.4 V	0.4 V
Maximum overshoot area above VDD	0.67 V-ns	0.5 V-ns	0.4 V-ns	0.33 V-ns

Table 28 AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask Pins

CK, $\overline{CK}$, DQ, DQS, $\overline{DQS}$, DM

Parameter	Specification			
	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600
Maximum peak amplitude allowed for overshoot area	0.4 V	0.4 V	0.4 V	0.4 V
Maximum overshoot area above VDDQ	0.25 V-ns	0.19 V-ns	0.15 V-ns	0.13 V-ns

PASS Condition

The measured maximum voltage value can be less than or equal to the maximum overshoot value.

The calculated Overshoot area value can be less than or equal to the maximum Overshoot area allowed.

Measurement Algorithm

1. Set the number of sampling points to 2M samples.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Calculate initial time scale value based on the number of sampling points.
4. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
5. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
6. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.

7 Initialize the scope settings.

8 Get timestamp of maximum peak voltage on the waveform.

9 Perform manual zoom waveform to maximum peak area.

10 Get the timestamp of voltage value for VDD(-1.8 V) level closest to the peak point value in order to calculate the maximum overshoot length duration.

11 Calculate the Overshoot area (V-ns)

   a Area of calculation is based on the area of calculation of a triangle where the Overshoot width is used as the triangle base and the Overshoot amplitude is used as the triangle height.

   b Area = 0.5 * base * height.

12 When multiple trials are performed, the largest value (worst case) among all the trials will be used as the test result for the Overshoot amplitude and Overshoot area. The worst case for the area might not happen during the worst case for the amplitude.

13 Compare test results against the compliance test limits.

Test References

See Table 37 - AC Overshoot/Undershoot Specification for Address and Control Pins, and Table 38 - AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask Pins, in the *JEDEC Standard JESD79-3*.

AC Undershoot Test Method of Implementation

The Undershoot Test can be divided into two sub-tests: Undershoot amplitude and Undershoot area. The purpose of this test is to verify that the undershoot value of the test signal is less than or equal to the conformance limit of the maximum peak amplitude allowed for undershoot as specified in the *JEDEC Standard JESD79-3*.

When there is an undershoot, the area is calculated based on the undershoot width. The Undershoot area should be less than or equal to the conformance limit of the maximum undershoot area allowed as specified in the *JEDEC Standard JESD79-3*.

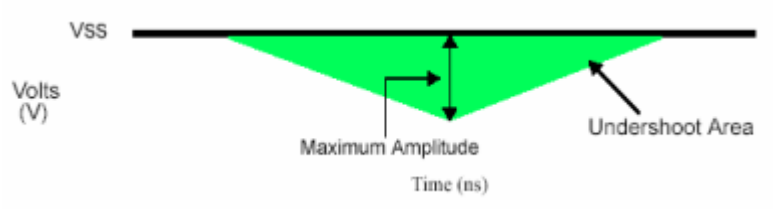


Figure 30 AC Undershoot

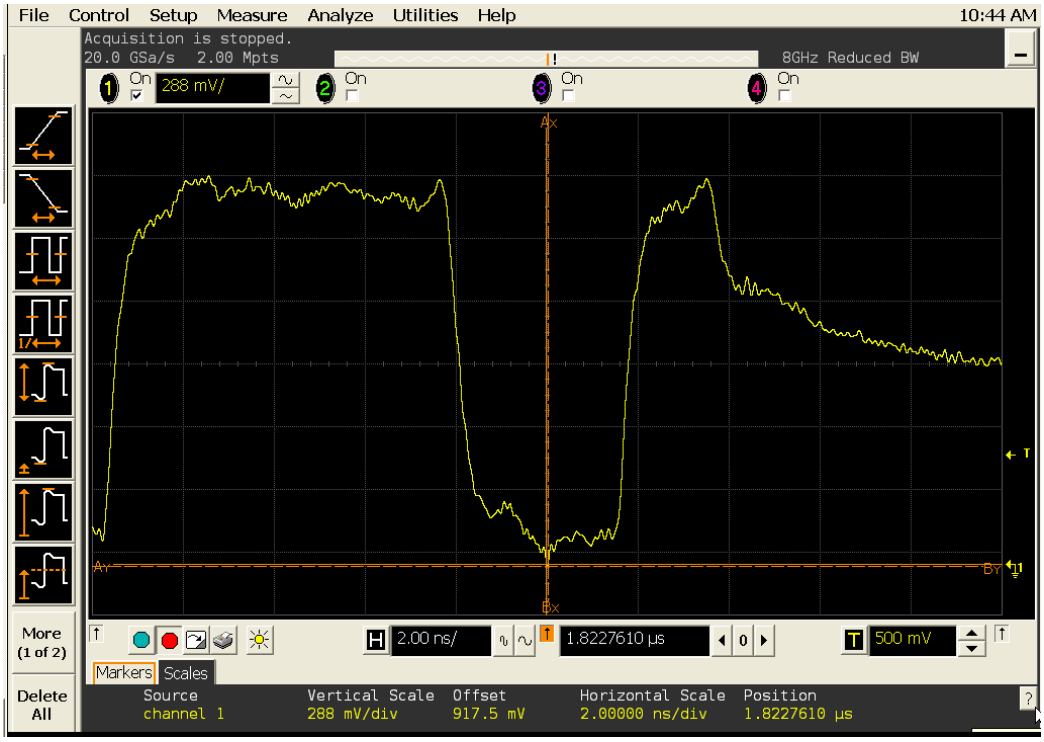


Figure 31 AC Undershoot in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal
- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)*
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

Test Definition Notes from the Specification

Table 29 AC Overshoot/Undershoot Specification for Address and Control Pins

A0-A15, BA0-BA3, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE, ODT

Parameter	Specification			
	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600
Maximum peak amplitude allowed for undershoot area	0.4 V	0.4 V	0.4 V	0.4 V
Maximum undershoot area above VDD	0.67 V-ns	0.5 V-ns	0.4 V-ns	0.33 V-ns

Table 30 AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask Pins

CK, $\overline{CK}$, DQ, DQS, $\overline{DQS}$, DM

Parameter	Specification			
	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600
Maximum peak amplitude allowed for undershoot area	0.4 V	0.4 V	0.4 V	0.4 V
Maximum undershoot area above VDDQ	0.25 V-ns	0.19 V-ns	0.15 V-ns	0.13 V-ns

PASS Condition

The measured minimum voltage value for the test signal can be less than or equal to the maximum undershoot value.

The calculated undershoot area value can be less than or equal to the maximum undershoot area allowed.

Measurement Algorithm

1. Set the number of sampling points to 2M samples.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Calculate initial time scale value based on the number of sampling points.
4. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
5. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
6. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
7. Initialize the scope settings.
8. Get timestamp of minimum peak voltage on the waveform.
9. Perform manual zoom waveform to minimum peak area.
10. Get timestamp of voltage value for GND (0 V) level closest to the minimum peak point value in order to calculate the undershoot length duration.
11. Calculate the Undershoot area (V-ns)
    a. Area of calculation is based on the area of calculation of a triangle where the undershoot width is used as the triangle base and the undershoot amplitude is used as the triangle height.
    b. Area = 0.5 * base * height.
12. When multiple trials are performed, the largest value (worst case) among all the trials will be used as the test result for the Undershoot amplitude and Undershoot area. The worst case for the area might not happen during the worst case for the amplitude.
13. Compare test results against the compliance test limits.

Test References

See Table 37 - AC Overshoot/Undershoot Specification for Address and Control Pins, and Table 38 - AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask Pins, in the *JEDEC Standard JESD79-3*.

7 Differential Signals AC Input Parameters Tests

This section provides the Methods of Implementation (MOIs) for Differential Signals AC Input tests using an Agilent 54850A series or 80000 series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR3 Compliance Test Application.

Probing for Differential Signals AC Input Parameters Tests

When performing the Differential Signals AC Input Parameters tests, the DDR3 Compliance Test Application will prompt you to make the proper connections. The connection for the Differential Signals AC Input Parameters tests may look similar to the following diagram. Refer to the Connection tab in DDR3 Electrical Performance Compliance application for the exact number of probe connections.

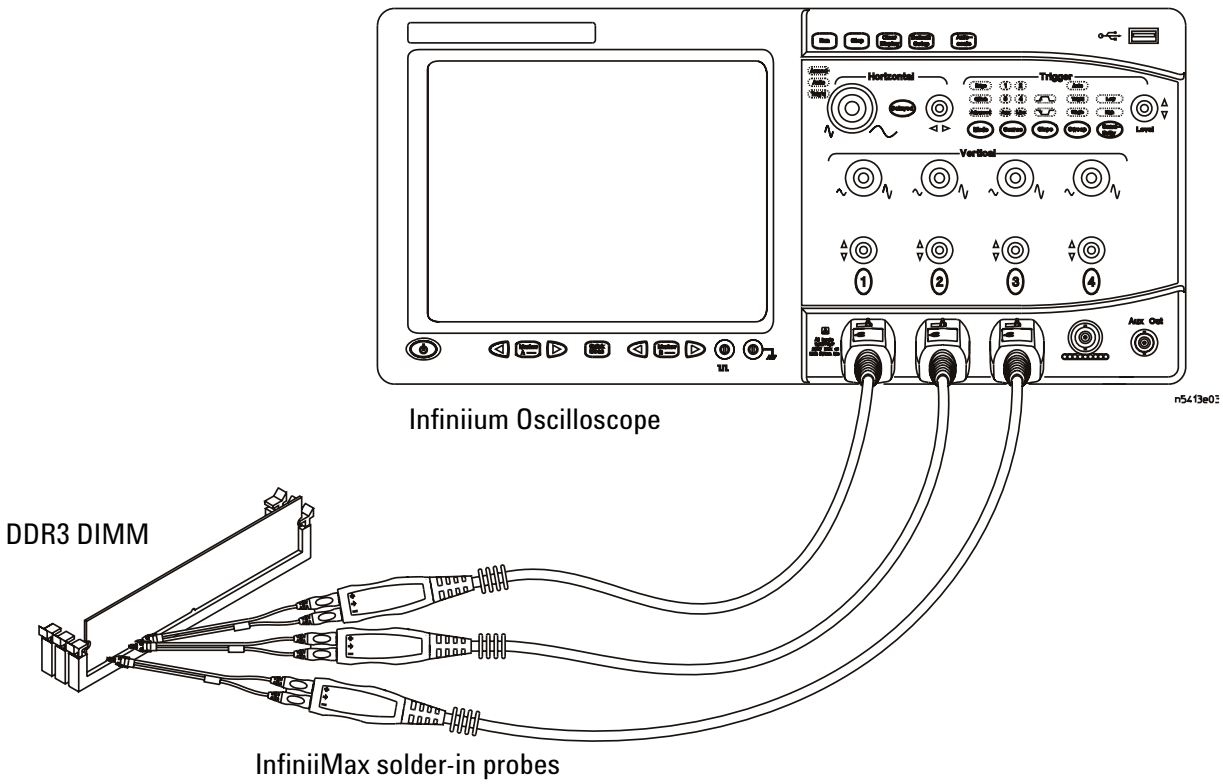


Figure 32 Probing for Differential Signals AC Input Parameters Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR3 Compliance Test Application. (The channels shown in Figure 32 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 16, “InfiniiMax Probing,” starting on page 261.

Test Procedure

1. Start the automated test application as described in “Starting the DDR3 Compliance Test Application" on page 27.
2. Ensure that the RAM reliability test software is running on the computer system where the DDR3 Device Under Test (DUT) is attached. This software will perform test on all unused RAM on the system by producing repetitive burst of read-write data signals to the DDR3 memory.
3. Connect the differential solder-in probe head to the PUTs on the DDR3 DIMM.
4. Connect the oscilloscope probes to any channels of the oscilloscope.
5. In the DDR3 Test application, click the Set Up tab.
6. Select the Speed Grade options. For Differential Signals AC Input Parameters Tests, you can select any speed grade within the selection: DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600.
7. Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.
8. Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

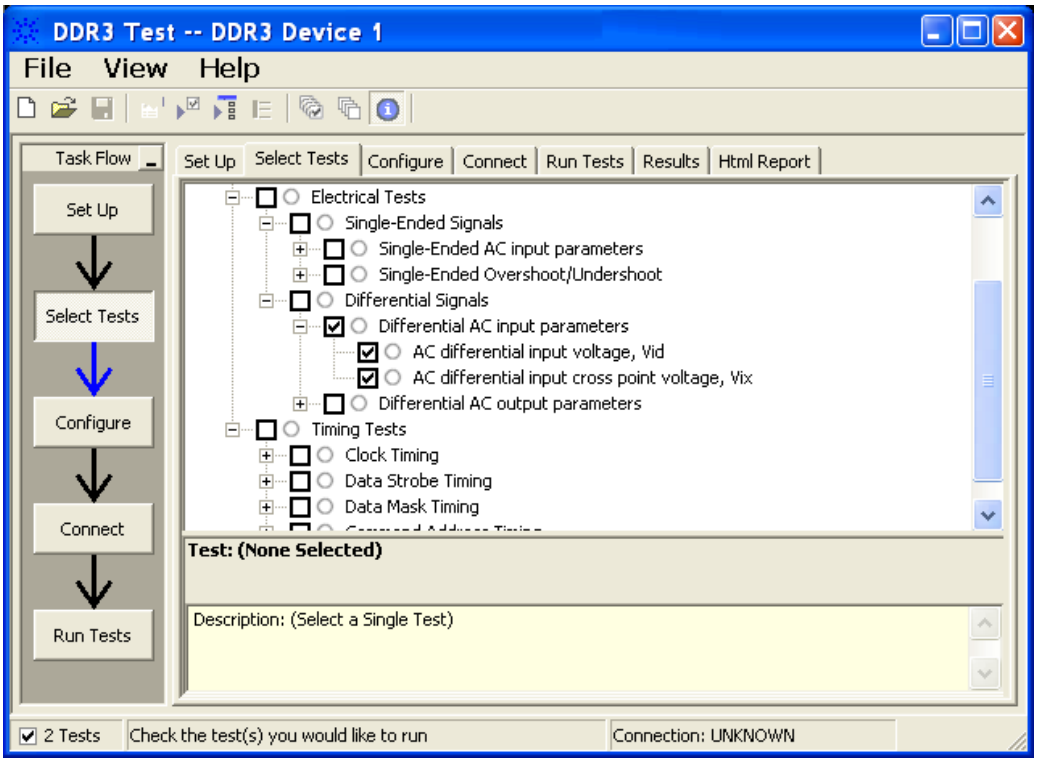


Figure 33 Selecting Differential Signals AC Input Parameters Tests

9 Follow the DDR3 Test application's task flow to set up the configuration options (see Table 31), run the tests and view the tests results.

Table 31 Test Configuration Options

Configuration Option	Description
Stop on error	Enabling this option will allow error messages to prompt whenever the test criteria is not met. Disabling this option will allow the system to bypass all the error messages that could occur and proceed to the next test. This option is suitable for long hours multiple trials.
Signal Threshold setting by percentage	This option allows you to define the Upper and Lower threshold of the signal by percentage.
VDD	Input supply voltage value.
VDDQ	Input supply voltage for data output.
Vref	Input reference voltage value.
Vih(DC)	Input voltage high value (direct current).
Vih(AC)	Input voltage high value (alternating current).
Vil(DC)	Input voltage low value (direct current).
Vil(AC)	Input voltage low value (alternating current).
InfiniiScan Limits	
Read Cycle	
IScan_UL_READ	Identifies the upper limit for Setup Time measurement used in the InfiniiScan Measurement Mode (READ cycle)
IScan_LL_READ	Identifies the lower limit for Setup Time measurement used in the InfiniiScan Measurement Mode (READ cycle)
Write Cycle	
IScan_UL_WRITE	Identifies the upper limit for Setup Time measurement used in the InfiniiScan Measurement Mode (WRITE cycle)
IScan_LL_WRITE	Identifies the lower limit for Setup Time measurement used in the InfiniiScan Measurement Mode (WRITE cycle)
Differential Tests	
Pin Under Test, PUT	Identifies the Pin Under Test for Differential AC parameters.
PUT (+) Source	Identifies the source of the PUT(+) for Differential AC tests.
PUT (-) Source	Identifies the source of the PUT(-) for Differential AC tests.
Supporting Pin	Identifies the required supporting pin for Differential AC parameters.
Supporting Pin Source	Identifies the source of the supporting pin for Differential AC tests.

$V_{ID(AC)}$, AC Differential Input Voltage - Test Method of Implementation

The purpose of this test is to verify that the magnitude difference between the differential input signals pair is within the conformance limits of the $V_{ID(AC)}$ as specified in the *JEDEC Standard JESD79-3*.

The value of V_{DDQ} which directly affects the conformance upper limit is defaulted to 1.8 V. However, users have the flexibility to change this value.

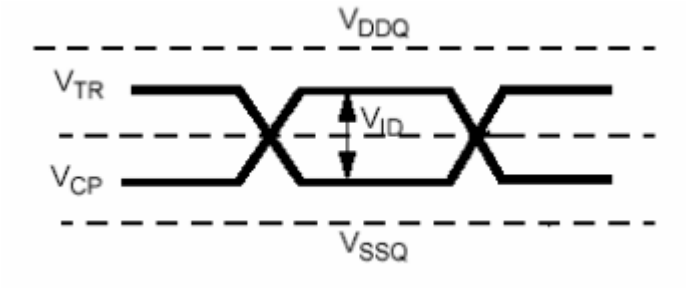


Figure 34 V_{ID} AC Differential Input Voltage

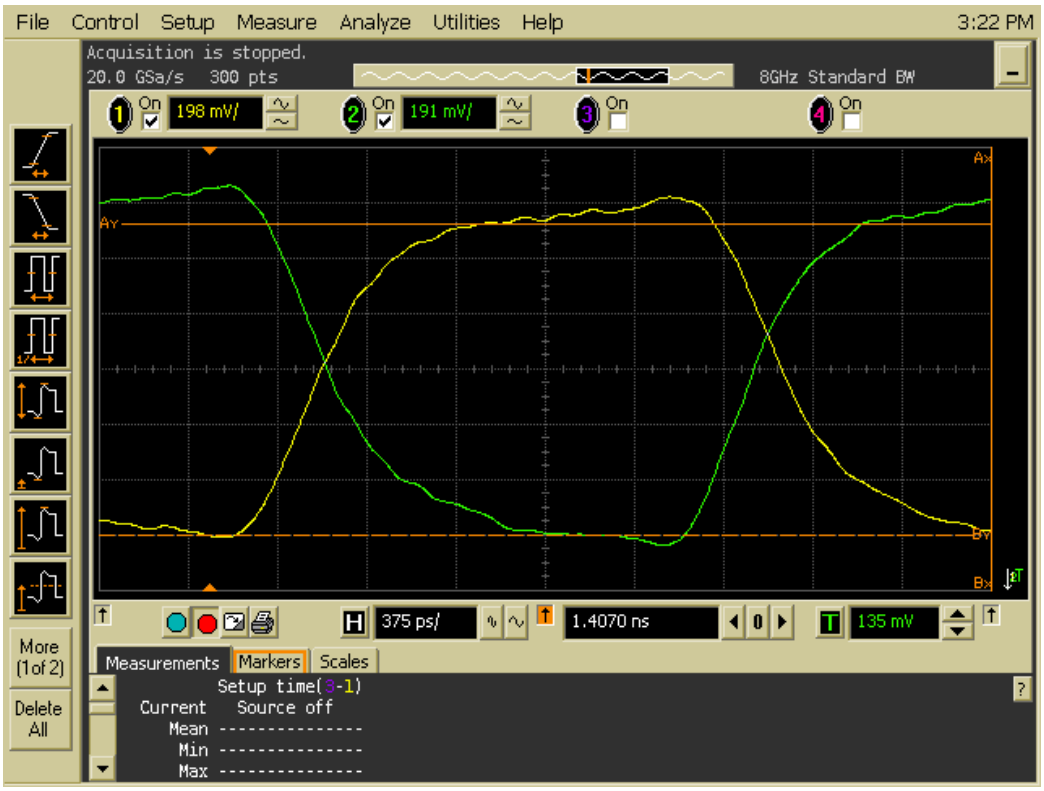


Figure 35 $V_{ID(AC)}$ in Infiniium oscilloscope.

Signals of Interest

Based on the test definition (Write cycle only):

- Data Strobe Signal OR
- Clock Signal

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)*
- Data Signal (DQ as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

Test Definition Notes from the Specification

Table 32 Differential AC and DC Input Levels

Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600		Units	Notes
		Min	Max		
V_{IHdiff}	Differential input logic high	+0.200	-	V	1
V_{ILdiff}	Differential input logic low	-	-0.200	V	1

NOTE 1: Refer to 8.6 Overshoot and Undershoot Specifications at page 113 in the *JEDEC Standard JESD79-3*.

PASS Condition

The calculated magnitude of the differential voltage for the test signals pair can be within the conformance limits of the $V_{ID(ac)}$ value.

Measurement Algorithm

1. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
2. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.

5 Obtain sample or acquire data waveforms, for example CK+ and CK-.

6 Use histogram function (mode value) to find the nominal high level value for CK+ and nominal low level value for CK-.

7 Subtract the CK- low level value from the CK+ high level value.

8 Compare test results against the compliance test limits.

Test References

See Table 27 - Differential AC and DC Input Levels, in the *JEDEC Standard JESD79-3*.

$V_{IX(AC)}$, AC Differential Input Cross Point Voltage -Test Method of Implementation

The purpose of this test is to verify the crossing point of the input differential test signals pair is within the conformance limits of the $V_{IX(AC)}$ as specified in the *JEDEC Standard JESD79-3*.

The value of V_{DDQ} which directly affects the conformance upper limit is defaulted to 1.8 V. However, users have the flexibility to change this value.

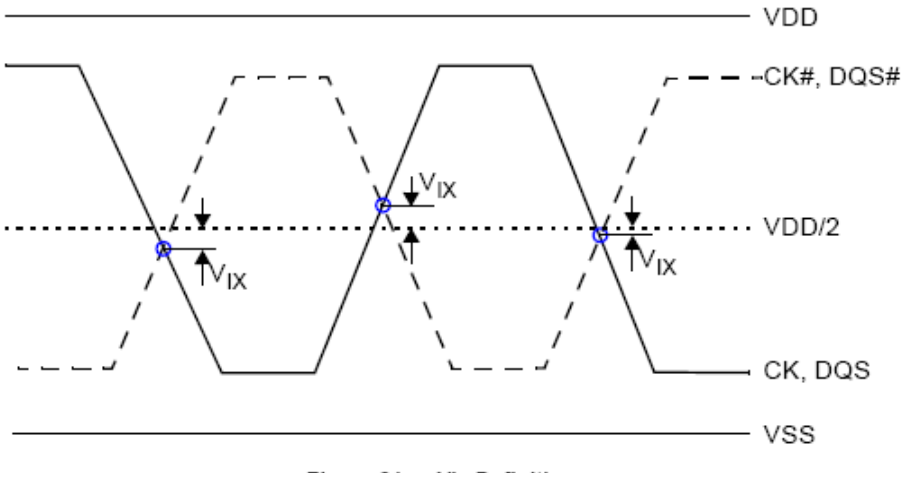


Figure 36 V_{IX} AC Differential Input Voltage

Figure 37 $V_{IX(AC)}$ in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Write cycle only):

- Data Strobe Signal OR
- Clock Signal

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)*
- Data Signal (DQ as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

Test Definition Notes from the Specification

Table 33 Cross Point Voltage for Differential Input Signals (CK, DQS)

Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600		Units
		Min	Max	
V_{IX}	Differential Input Cross Point Voltage relative to VDD/2	-150	150	mV

PASS Condition

The measured crossing point value for the differential test signals pair can be within the conformance limits of $V_{IX(AC)}$ value.

Measurement Algorithm

1. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
2. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Obtain sample or acquire data waveforms, for example CK+ and CK-.
6. Generate the differential waveform from two source input.
7. Get the timestamp of voltage value = 0 V level (crossing point).
8. Get the actual crossing value using the obtained timestamp.
9. Compare test results against the compliance test limits.

Test References

See Table 28 - Cross Point Voltage for Differential Input Signals (CK, DQS), in the *JEDEC Standard JESD79-3*.

7 Differential Signals AC Input Parameters Tests

8 Differential Signal AC Output Parameters Tests

This section provides the Methods of Implementation (MOIs) for Differential Signals AC Output tests using an Agilent 54850A series or 80000 series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR3 Compliance Test Application.

Probing for Differential Signals AC Output Parameters Tests

When performing Differential Signals AC Input Parameters tests, the DDR3 Compliance Test Application will prompt you to make the proper connections. The connection for Differential Signals AC Output Parameters tests may look similar to below diagram. Refer to the Connection tab in DDR3 Electrical Performance Compliance application for the exact number of probe connections.

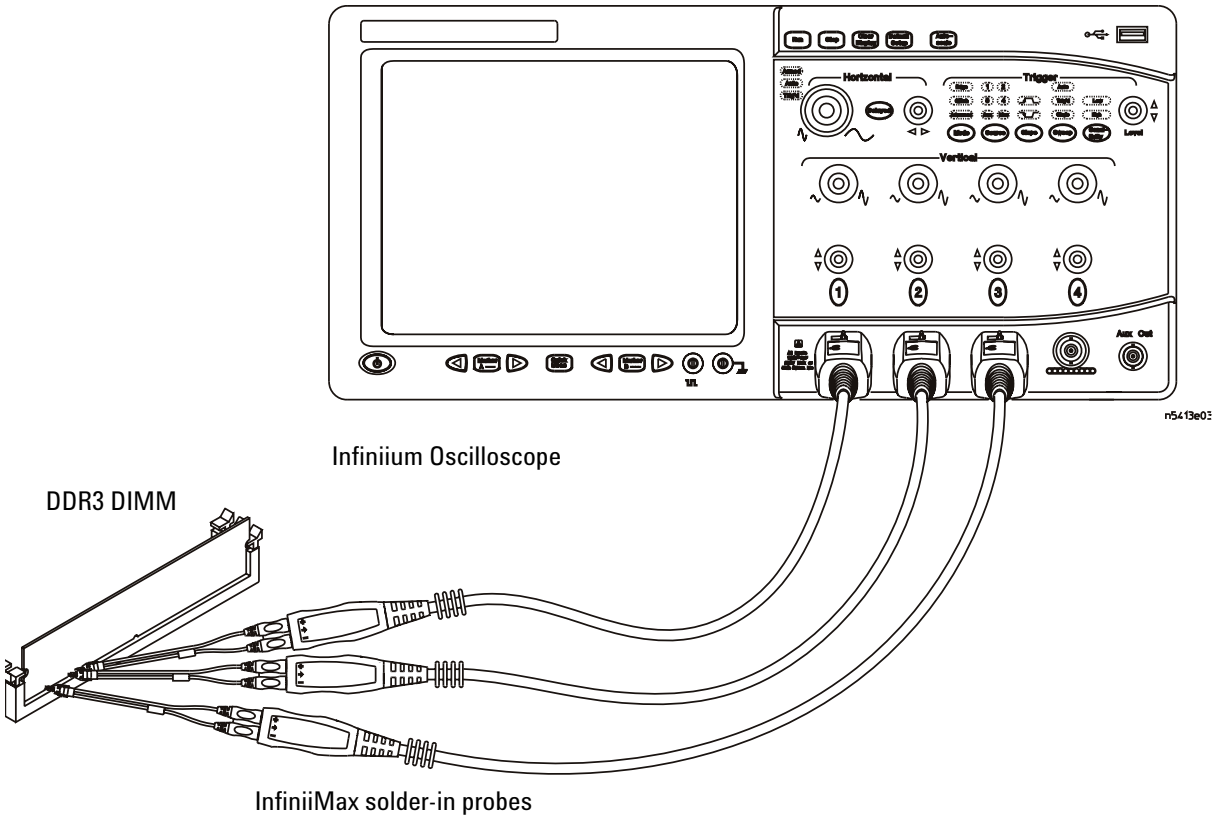


Figure 38 Probing for Differential Signals AC Output Parameters Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR3 Compliance Test Application. (The channels shown in Figure 38 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 16, “InfiniiMax Probing,” starting on page 261.

Test Procedure

1. Start the automated test application as described in “Starting the DDR3 Compliance Test Application" on page 27.
2. Ensure that the RAM reliability test software is running on the computer system where the DDR3 Device Under Test (DUT) is attached. This software will perform test on all the unused RAM on the system by producing repetitive burst of read-write data signals to the DDR3 memory.
3. Connect the differential solder-in probe head to the PUTs on the DDR3 DIMM.k
4. Connect the oscilloscope probes to any channels of the oscilloscope.
5. In the DDR3 Test application, click the Set Up tab.
6. Select the Speed Grade options. For Differential Signals AC Output Parameters Tests, you can select any speed grade within the selection: DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600.
7. Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.
8. Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

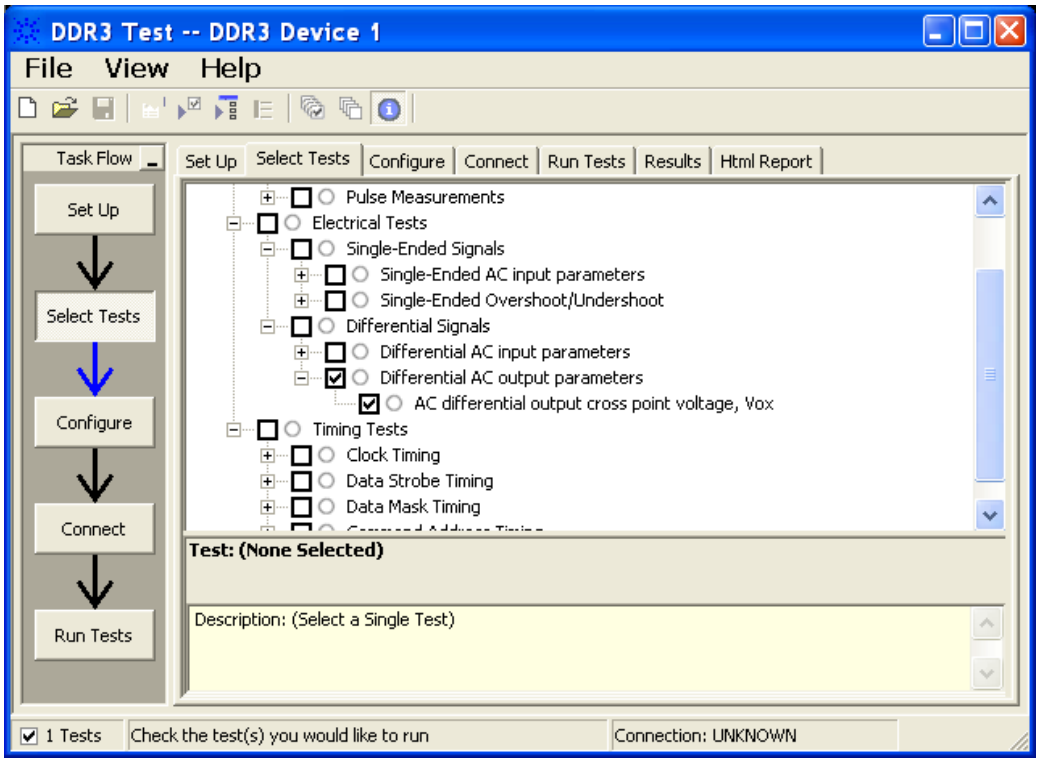


Figure 39 Selecting Differential Signals AC Output Parameters Tests

9 Follow the DDR3 Test application's task flow to set up the configuration options (see Table 34), run the tests and view the tests results.

Table 34 Test Configuration Options

Configuration Option	Description
Stop on error	Enabling this option will allow error messages to prompt whenever the test criteria is not met. Disabling this option will allow the system to bypass all the error messages that could occur and proceed to the next test. This option is suitable for long hours multiple trials.
Signal Threshold setting by percentage	This option allows you to define the Upper and Lower threshold of the signal by percentage.
VDD	Input supply voltage value.
VDDQ	Input supply voltage for data output.
Vref	Input reference voltage value.
Vih(DC)	Input voltage high value (direct current).
Vih(AC)	Input voltage high value (alternating current).
Vil(DC)	Input voltage low value (direct current).
Vil(AC)	Input voltage low value (alternating current).
InfiniiScan Limits	
Read Cycle	
IScan_UL_READ	Identifies the upper limit for Setup Time measurement used in the InfiniiScan Measurement Mode (READ cycle)
IScan_LL_READ	Identifies the lower limit for Setup Time measurement used in the InfiniiScan Measurement Mode (READ cycle)
Write Cycle	
IScan_UL_WRITE	Identifies the upper limit for Setup Time measurement used in the InfiniiScan Measurement Mode (WRITE cycle)
IScan_LL_WRITE	Identifies the lower limit for Setup Time measurement used in the InfiniiScan Measurement Mode (WRITE cycle)
Differential Tests	
Pin Under Test, PUT	Identifies the Pin Under Test for Differential AC parameters.
PUT (+) Source	Identifies the source of the PUT(+) for Differential AC tests.
PUT (-) Source	Identifies the source of the PUT(-) for Differential AC tests.
Supporting Pin	Identifies the required supporting pin for Differential AC parameters.
Supporting Pin Source	Identifies the source of the supporting pin for Differential AC tests.

V_{OX}, AC Differential Output Cross Point Voltage - Test Method of Implementation

The purpose of this test is to verify the crossing point of the output differential test signals pair is within the conformance limits of the $V_{OX(ac)}$ as specified in the *JEDEC Standard JESD79-3*.

The value of V_{DDQ} which directly affects the conformance upper limit is defaulted to 1.8 V. However, users have the flexibility to change this value.

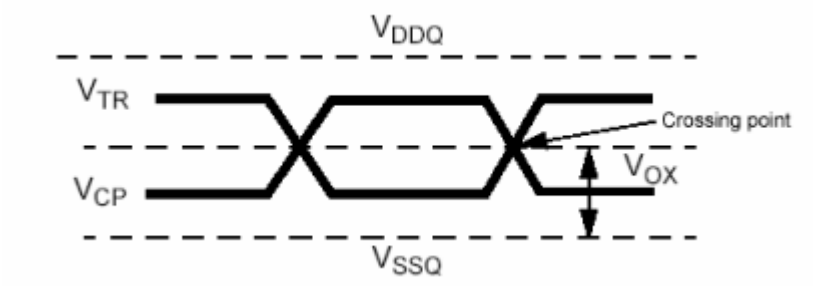


Figure 40 V_{OX} AC Differential Cross Point Voltage

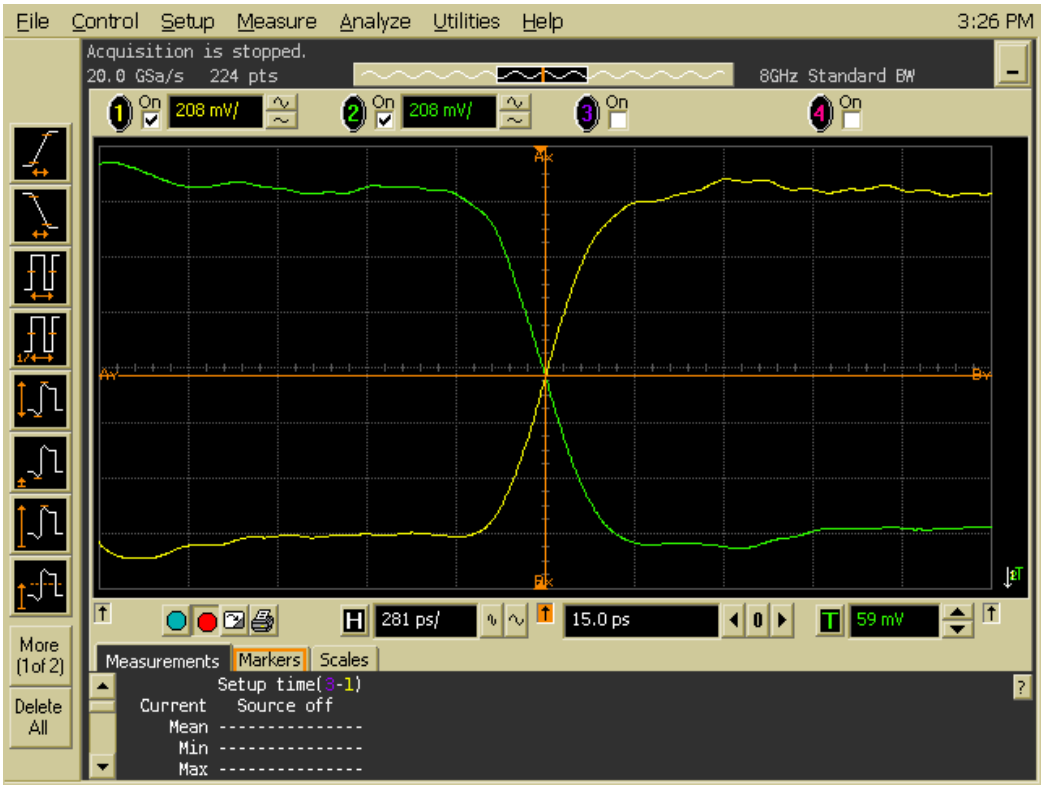


Figure 41 V_{OX} in Infiniium oscilloscope.

Signals of Interest

Based on the test definition (Read cycle only):

- Data Strobe Signal

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

Test Definition Notes from the Specification

-

PASS Condition

The measured crossing point value for the differential test signals pair can be within the conformance limits of $V_{OX(ac)}$ value.

Measurement Algorithm

1. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
2. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Obtain sample or acquire data waveforms, for example CK+ and CK-.
6. Generate the differential waveform from two source input.
7. Get the timestamp of voltage value = 0 V level (crossing point).
8. Get the actual crossing value using the obtained timestamp.
9. Compare test results against the compliance test limits.

Test References

-

9 Clock Timing (CT) Tests

This section provides the Methods of Implementation (MOIs) for Clock Timing tests using an Agilent 54850A series or 80000 series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR3 Compliance Test Application.

NOTE Both XYZ# and $\overline{\text{XYZ}}$ are referring to compliment. Thus, CK# is the same as $\overline{\text{CK}}$.

Probing for Clock Timing Tests

When performing the Clock Timing tests, the DDR3 Compliance Test Application will prompt you to make the proper connections. The connection for Clock Timing tests may look similar to the following diagram. Refer to the Connection tab in DDR3 Electrical Performance Compliance Test application for the exact number of probe connections. Typically, you need minimum three probe connections to run the tests.

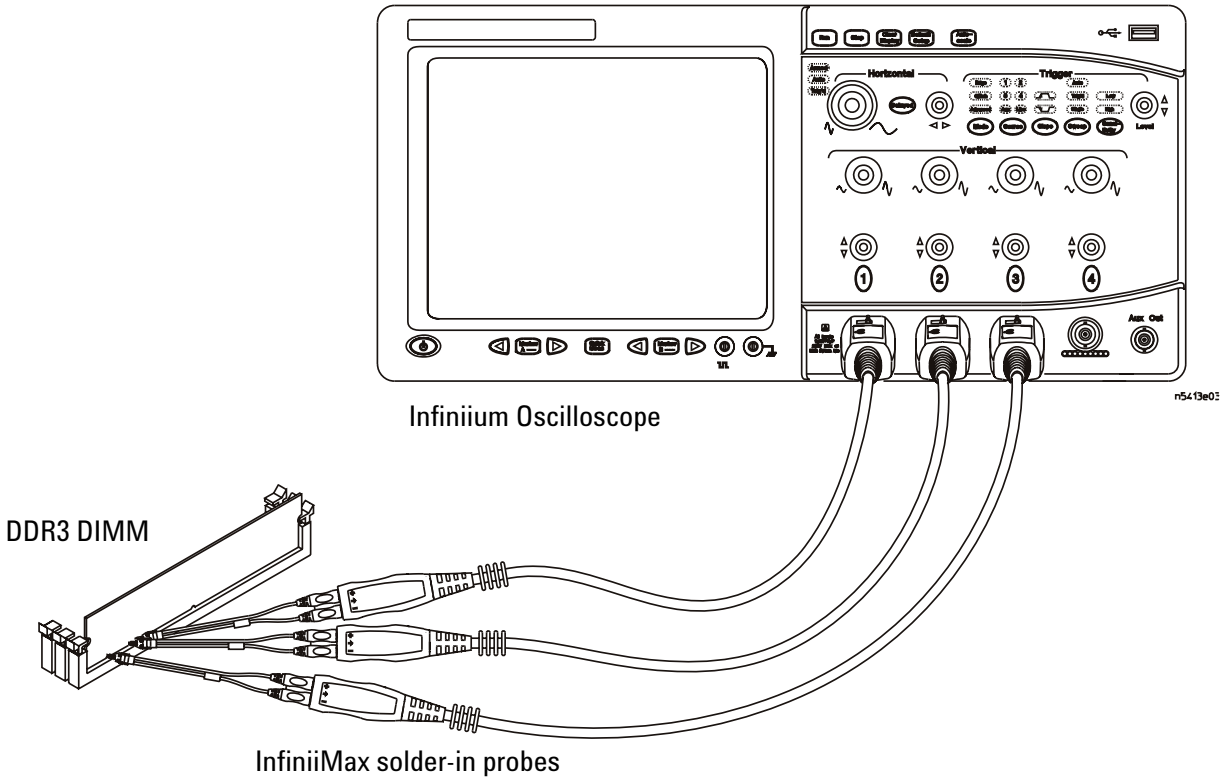


Figure 42 Probing for Clock Timing Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR3 Compliance Test Application. (The channels shown in Figure 42 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 16, “InfiniiMax Probing,” starting on page 261.

Test Procedure

1 Start the automated test application as described in “Starting the DDR3 Compliance Test Application" on page 27.

2 Ensure that the RAM reliability test software is running on the computer system where the DDR3 Device Under Test (DUT) is attached. This software will perform test on all the unused RAM on the system by producing repetitive burst of read-write data signals to the DDR3 memory.

3 Connect the differential solder-in probe head to the PUTs on the DDR3 DIMM.

4 Connect the oscilloscope probes to any channels of the oscilloscope.

5 In the DDR3 Test application, click the Set Up tab.

6 Select the Speed Grade options. For Clock Timing Tests, you can select any speed grade within the selection: DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

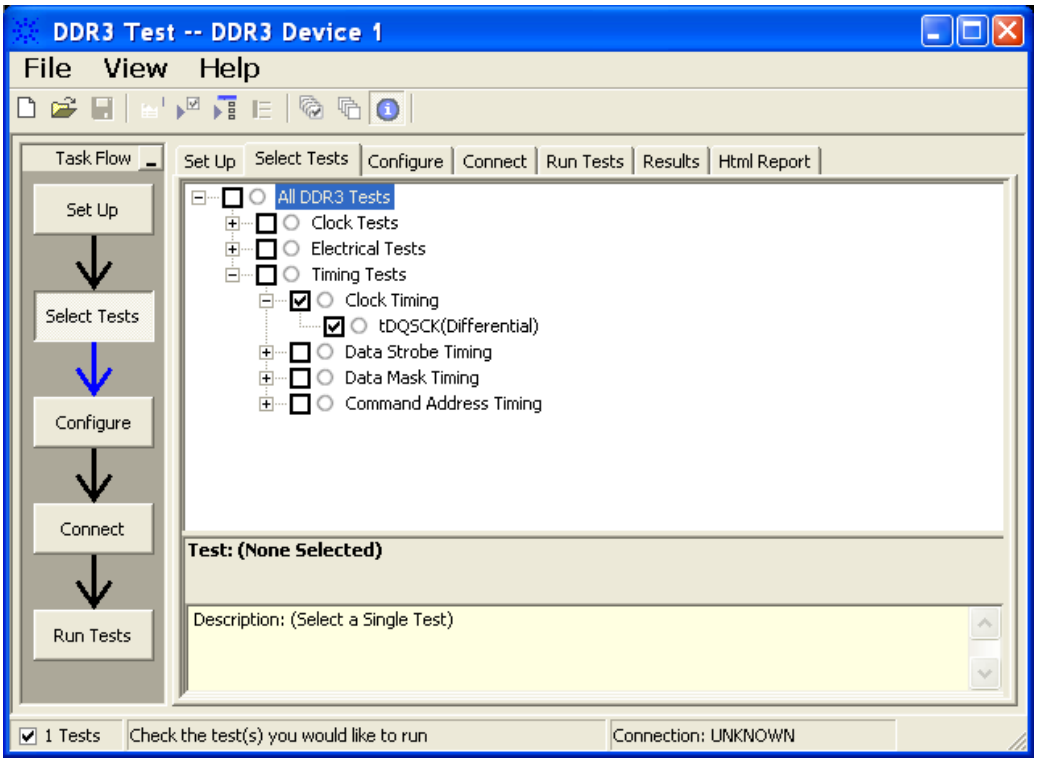


Figure 43 Selecting Clock Timing Tests

9 Follow the DDR3 Test application's task flow to set up the configuration options (see Table 35), run the tests and view the tests results.

Table 35 Test Configuration Options

Configuration Option	Description
Stop on error	Enabling this option will allow error messages to prompt whenever the test criteria is not met. Disabling this option will allow the system to bypass all the error messages that could occur and proceed to the next test. This option is suitable for long hours multiple trials.
Signal Threshold setting by percentage	This option allows you to define the Upper and Lower threshold of the signal by percentage.
VDD	Input supply voltage value.
VDDQ	Input supply voltage for data output.
Vref	Input reference voltage value.
Vih(DC)	Input voltage high value (direct current).
Vih(AC)	Input voltage high value (alternating current).
Vil(DC)	Input voltage low value (direct current).
Vil(AC)	Input voltage low value (alternating current).
Timing Tests	
Total Bit Display	Allows you to select the number of data bits to be displayed at the end of the test. Selecting more bits gives a better view of the entire burst of signals.
Verify Selected Rank Only?	If you choose Yes, you require an additional channel for the Chip Select (CS). Measurement will only be done on the selected rank based on the Chip Select signal connected to the oscilloscope.
Channel (1,2,3)	Signal connected to the specific channel.
Pin Under Test, PUT	Signal used for testing.

tDQSCK, DQS Output Access Time from CK/CK #- Test Method of Implementation

The purpose of this test is to verify that the time interval from the data strobe output (DQS rising and falling edge) access time to the nearest rising or falling edge of the clock is within the conformance limit as specified in the *JEDEC Standard JESD79-3*.

There is tDQSCK(min) and tDQSCK(max) as shown in Figure 44 and Figure 45. From the specification, you can observe that the minimum value is at negative while the maximum is at positive.

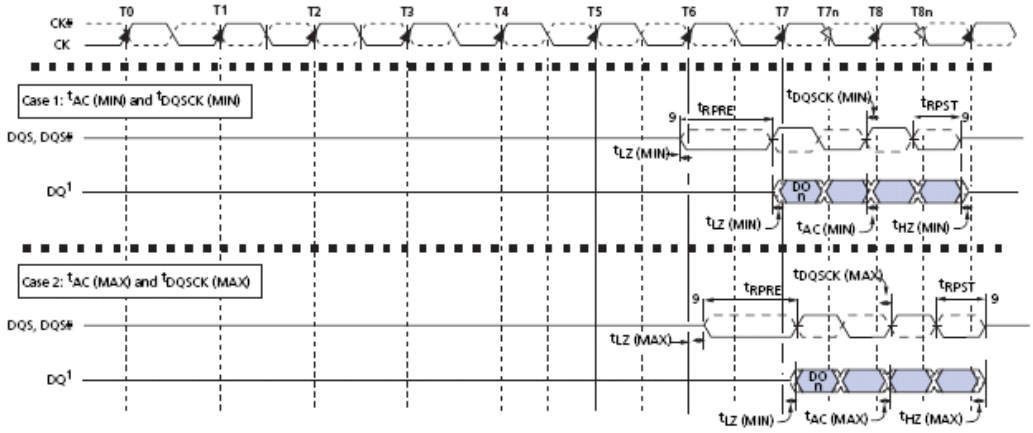


Figure 44 DQS Output Access Time from CK/CK#

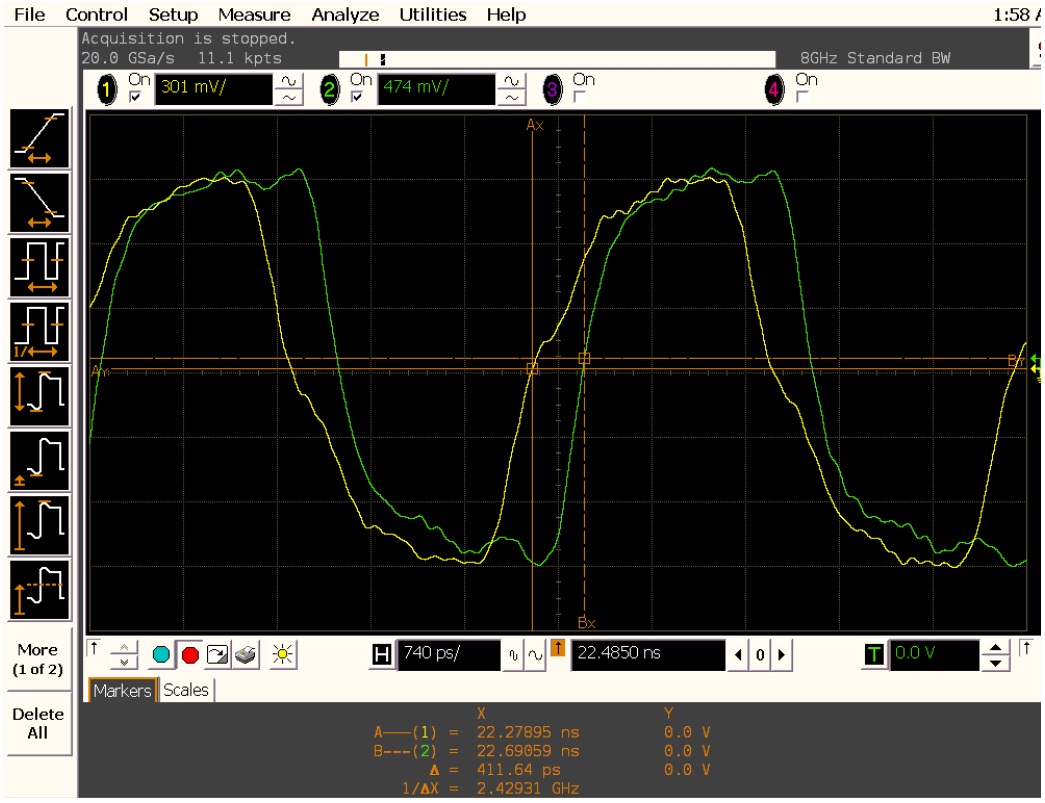


Figure 45 tDQSCK in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Read cycle only):

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 36 DQS Output Access Time Test

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# rising edge output access time from CK/CK#	tDQSCK	-350	350	-265	265	ps	12,13

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# rising edge output access time from CK/CK#	tDQSCK	-225	225	-200	200	ps	12,13

NOTE 12: Please refer to page 161, *JEDEC Standard JESD79-3*.

NOTE 13: Please refer to page 172, *JEDEC Standard JESD79-3*.

PASS Condition

The measured time interval between the data strobe access output and the rising edge of the clock should be within the specification limit.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope setting. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
6. Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.
7. If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.

8 Search for the DQS preamble towards the left from the point where the Read cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.

9 Once the preamble is located, call the “BinaryEdgeNormal” function to obtain the Edge number. This Edge number will be used to locate the point of interest on the specific signal.

10 After obtaining the Edge number for the respective signal, begin the tDQSCK measurement bit by bit in the Read data burst. Begin at the 1st bit of the Read cycle, from the Read preamble.

11 Continue the measurement until last bit (for example, until a tristate happens, which indicates the end of a data burst for the respective Read cycle).

12 The DQS-Clock timing measurement compares the rising edge (DQS crossing against clock crossing) OR the falling edge (DQS crossing against clock crossing).

13 Within the data burst, measure each bit, for instance the rising and falling edge of the DQS-Clock. Capture the worst case data each time a new value is measured.

14 Once all bits are validated, assign marker A for the clock signal while marker B for the data signal, for the worst case bit.

15 Measure delta of marker A and marker B and this will be the test result.

16 Compare the test result against the compliance test limit.

Test References

See Table 66 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79-3*.

10 Data Strobe Timing (DST) Tests

This section provides the Methods of Implementation (MOIs) for Data Strobe Timing tests using an Agilent 54850A series or 80000 series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR3 Compliance Test Application.

NOTE Both XYZ# and $\overline{\text{XYZ}}$ are referring to compliment. Thus, CK# is the same as $\overline{\text{CK}}$.

Probing for Data Strobe Timing Tests

When performing the Data Strobe Timing tests, the DDR3 Compliance Test Application will prompt you to make the proper connections. The connection for Data Strobe Timing tests may look similar to the following diagram. Refer to the Connection tab in DDR3 Electrical Performance Compliance Test application for the exact number of probe connections. Typically, you need minimum three probe connections to run the tests.

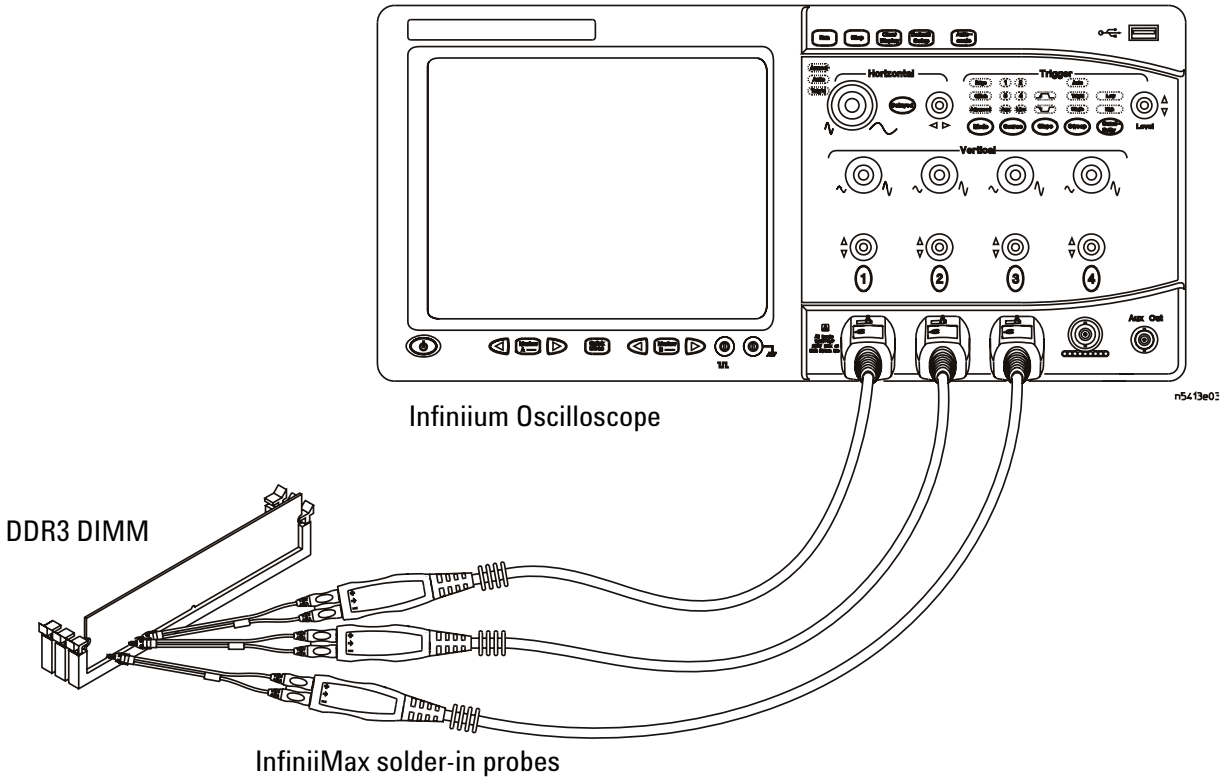


Figure 46 Probing for Data Strobe Timing Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR3 Compliance Test Application. (The channels shown in Figure 46 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 16, “InfiniiMax Probing,” starting on page 261.

Test Procedure

1 Start the automated test application as described in “Starting the DDR3 Compliance Test Application" on page 27.

2 Ensure that the RAM reliability test software is running on the computer system where the DDR3 Device Under Test (DUT) is attached. This software will perform test on all the unused RAM on the system by producing repetitive burst of read-write data signals to the DDR3 memory.

3 Connect the differential solder-in probe head to the PUTs on the DDR3 DIMM.

4 Connect the oscilloscope probes to any channels of the oscilloscope.

5 In the DDR3 Test application, click the Set Up tab.

6 Select the Speed Grade options. For Clock Timing Tests, you can select any speed grade within the selection: DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

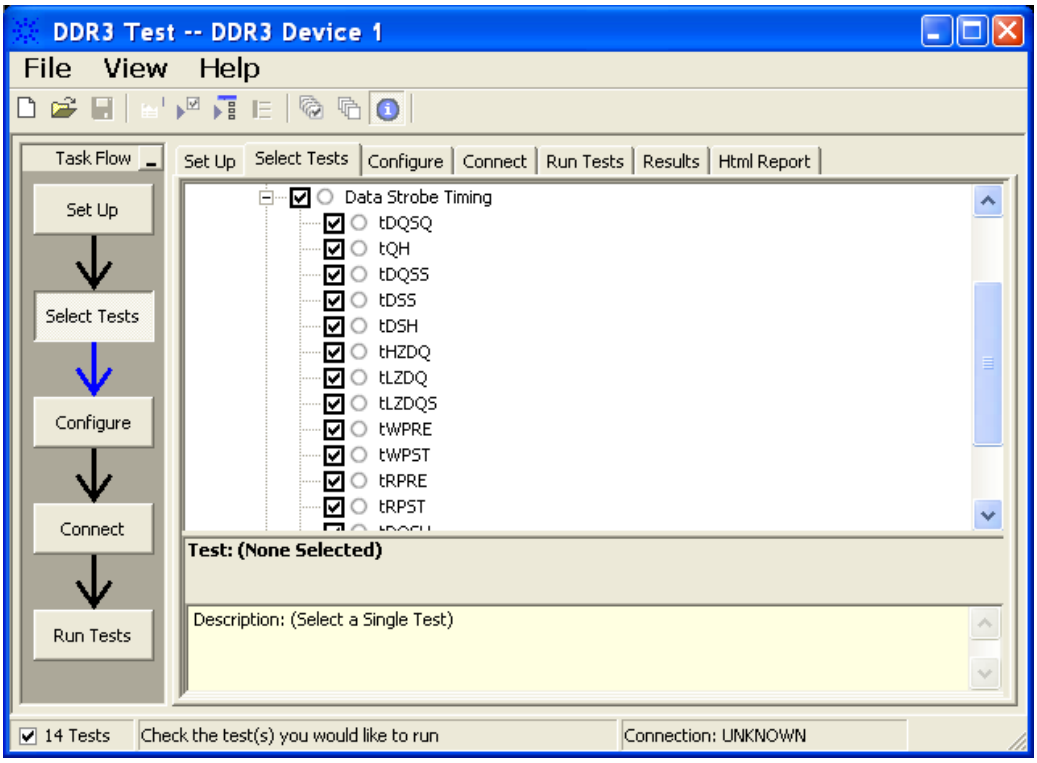


Figure 47 Selecting Data Strobe Timing Tests

9 Follow the DDR3 Test application's task flow to set up the configuration options (see Table 37), run the tests and view the tests results.

Table 37 Test Configuration Options

Configuration Option	Description
Stop on error	Enabling this option will allow error messages to prompt whenever the test criteria is not met. Disabling this option will allow the system to bypass all the error messages that could occur and proceed to the next test. This option is suitable for long hours multiple trials.
Signal Threshold setting by percentage	This option allows you to define the Upper and Lower threshold of the signal by percentage.
VDD	Input supply voltage value.
VDDQ	Input supply voltage for data output.
Vref	Input reference voltage value.
Vih(DC)	Input voltage high value (direct current).
Vih(AC)	Input voltage high value (alternating current).
Vil(DC)	Input voltage low value (direct current).
Vil(AC)	Input voltage low value (alternating current).
Timing Tests	
Total Bit Display	Allows you to select the number of data bits to be displayed at the end of the test. Selecting more bits gives a better view of the entire burst of signals.
Verify Selected Rank Only?	If you choose Yes, you require an additional channel for the Chip Select (CS). Measurement will only be done on the selected rank based on the Chip Select signal connected to the oscilloscope.
Channel (1,2,3)	Signal connected to the specific channel.
Pin Under Test, PUT	Signal used for testing.

tHZ(DQ), DQ Out High Impedance Time From CK/CK# - Test Method of Implementation

The purpose of this test is to verify that the time when the DQ is no longer driving (from high state OR low state to the high impedance stage), to the clock signal crossing, is within the conformance limits as specified in the *JEDEC Standard JESD79-3*.

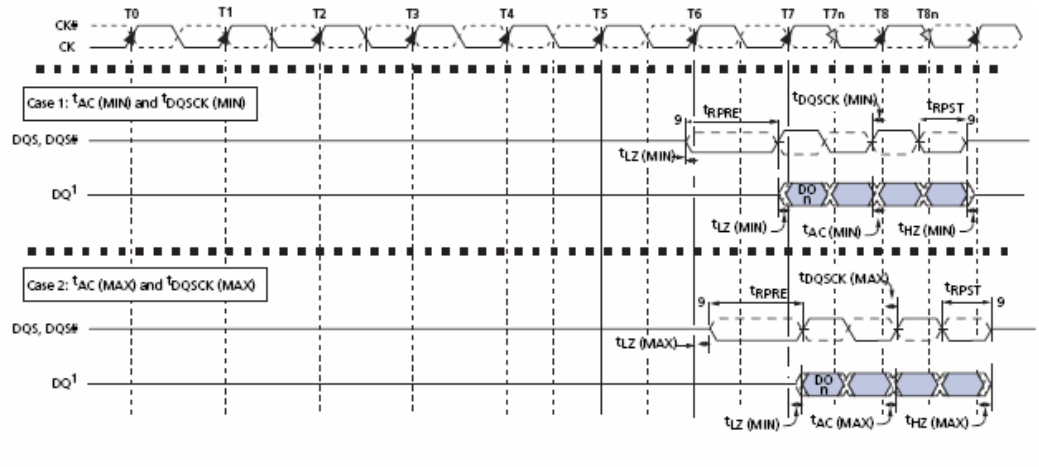


Figure 48 DQ Out High Impedance Time From CK/CK#

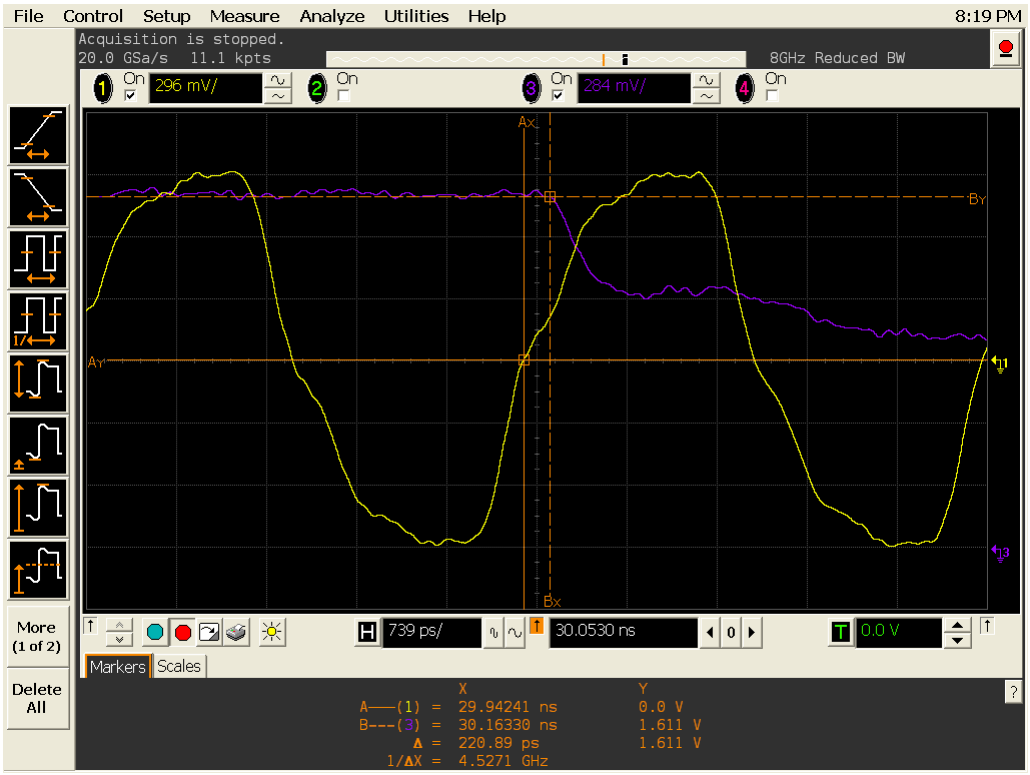


Figure 49 tHZ(DQ) in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Read cycle only):

- Data Signal (DQ as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 38 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
DQ high impedance time from CK/$\overline{CK}$	tHZ(DQ)	-	400	-	300	ps	12,13,14

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
DQ high impedance time from CK/$\overline{CK}$	tHZ(DQ)	-	250	-	225	ps	12,13,14

NOTE 12,13,14: Please refer to page 160, *JEDEC Standard JESD79-3*.

PASS Condition

The measured time interval from the point where the DQ starts to transit from high/low state to high impedance state, to the clock signal crossing point should be within the specification limit.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
6. Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.
7. If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.
8. Search for the DQS preamble towards the right from the point where the Read cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.

9 Once the preamble is located, call the “BinaryEdgeNormal” function, using Clock as the reference to define the Histogram Window for the DQ signal.

10 The Histogram Window is required to cover the DQ signal from the high/low state to the moment it starts to turn off the driver into tristate.

11 Setup the threshold value and measurement point for the DQ signal based on the histogram result.

12 Once all the points are obtained, proceed with the trigonometry calculation to find the point where the DQ starts to transit from high/low to the time when it turned off its driver into tristate.

13 Assign marker A for the clock signal crossing point while marker B for the data signal start to turn off its driver.

14 Measure delta of marker A and marker B and this will be the test result.

15 Compare the test result against the compliance test limit.

NOTE Some designs do not have tristate at V_{REF} (for example, 0.9V). This test is not guaranteed when this scenario happens, as there is no significant point of where the driver has been turned-off.

Test References

See Table 66 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79-3*.

tLZ(DQS), DQS Low-Impedance Time from CK/CK# - Test Method of Implementation

The purpose of this test is to verify that the time when the DQS starts driving (from tristate to high/low state) to the clock signal crossing, is within the conformance limit as specified in the *JEDEC Standard JESD79-3*.

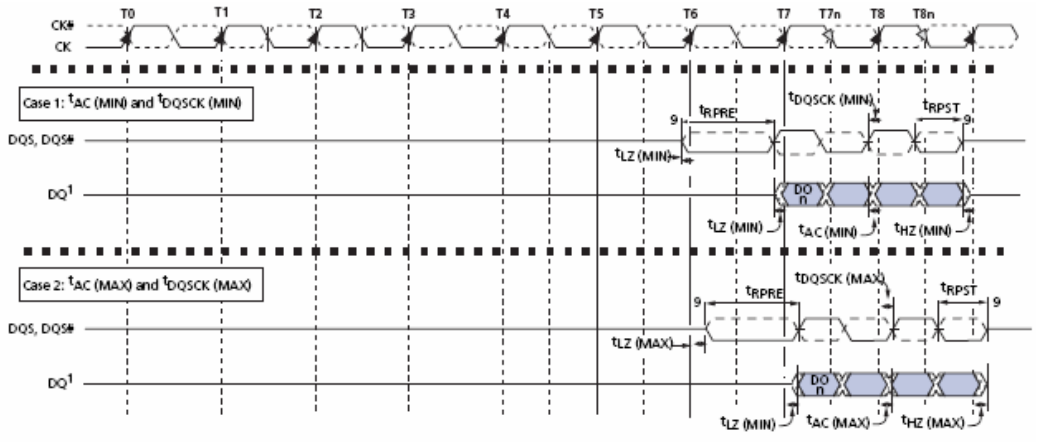


Figure 50 DQS Low-Impedance Time From CK/CK#

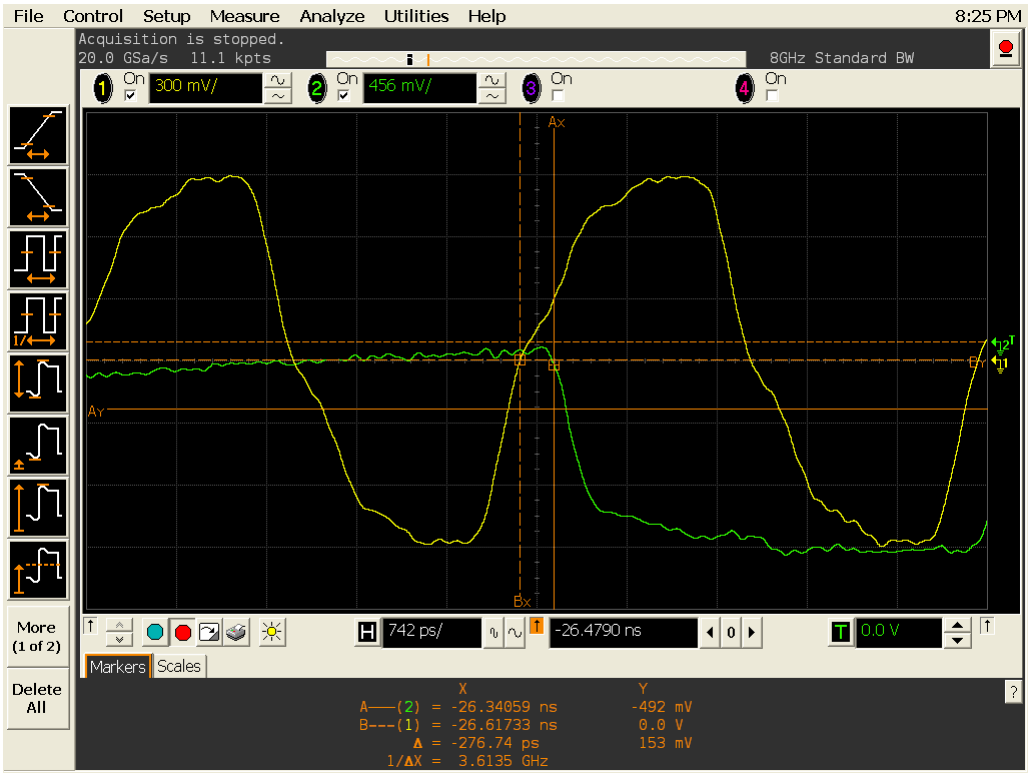


Figure 51 tLZ(DQS) in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Read cycle only):

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 39 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
DQS and DQS# low impedance time	tLZ(DQS)	-800	400	-600	300	ps	12,13,14

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
DQS and DQS# low impedance time	tLZ(DQS)	-500	250	-450	225	ps	12,13,14

NOTE 12,13,14: Please refer to page 160, *JEDEC Standard JESD79-3*.

PASS Condition

The measured time interval from the point where the DQS starts to transit from tristate to the moment when it starts to drive high/low (high impedance state to high/low state) to the clock signal crossing point, should be within the specification limit.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
6. Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.
7. If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.
8. Search for the DQS preamble towards the left from the point where the Read cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.

9 Once the preamble is located, call the “BinaryEdgeNormal” function, using the Clock as the reference to define the Histogram Window for the DQS signal.

10 The Histogram Window is required to cover the DQS signal from tristate to the moment it starts to drive the signal high/low.

11 Setup the threshold value and measurement point for the DQS signal based on the histogram result.

12 Once all the points are obtained, proceed with the trigonometry calculation to find the point where the DQS starts to transit from tristate to the time when it start to drive high/low.

13 Assign marker A for the clock signal crossing point while marker B for the data signal start to drive.

14 Measure delta of marker A and marker B and this will be the test result.

15 Compare the test result against the compliance test limit.

Test References

See Table 66 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79-3*.

tLZ(DQ), DQ Low-Impedance Time from CK/CK# - Test Method of Implementation

The purpose of this test is to verify that the time when the DQ starts driving (from high impedance state to high/low state), to the clock signal crossing, is within the conformance limit as specified in the *JEDEC Standard JESD79-3*.

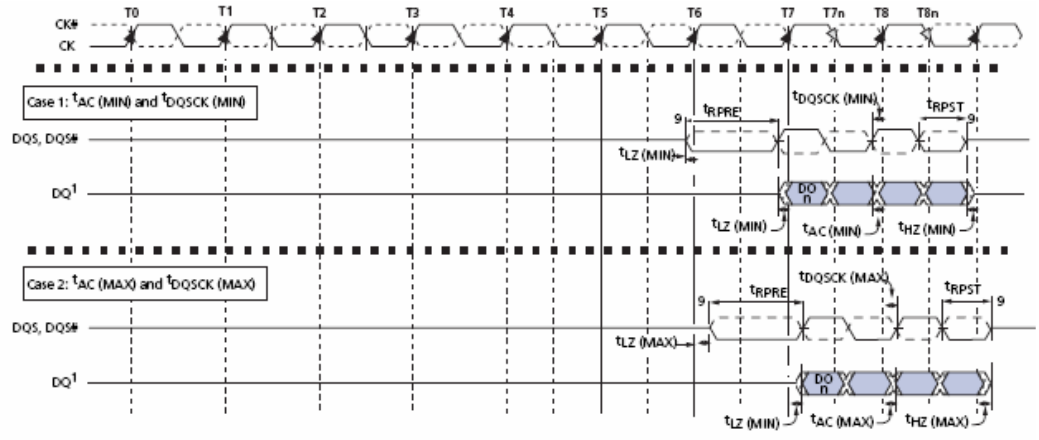


Figure 52 DQ Low-Impedance Time from CK/CK#

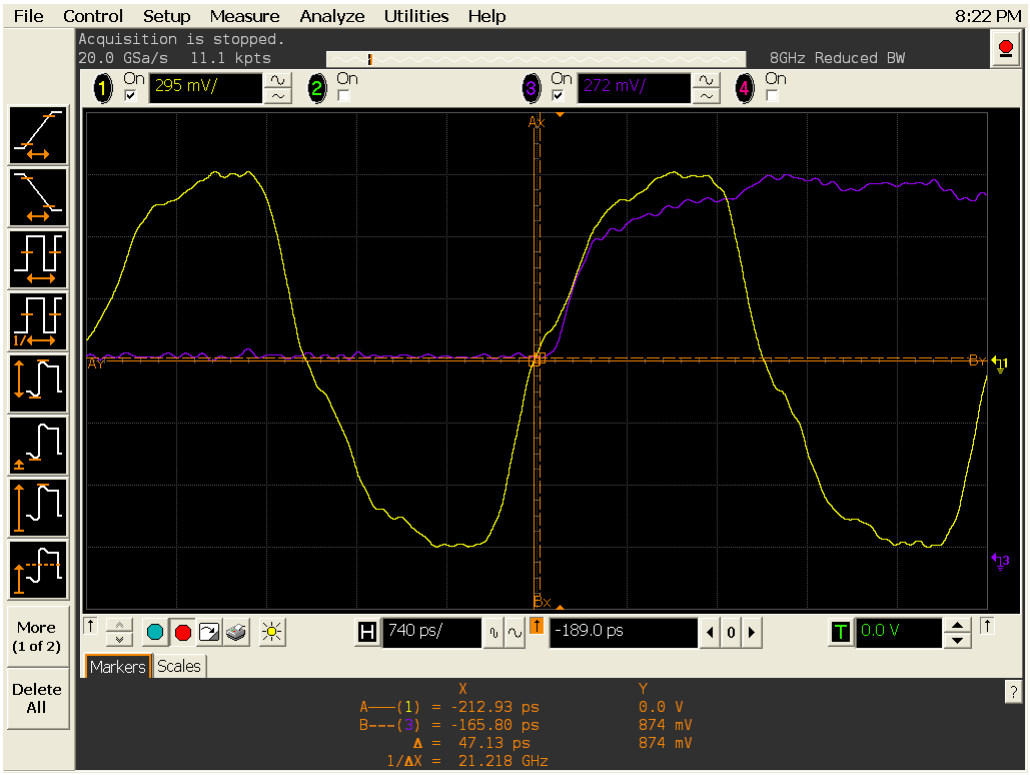


Figure 53 tLZ(DQ) in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Read cycle only):

- Data Signal (DQ as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 40 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
DQ low impedance time from CK/CK#	tLZ(DQ)	-800	400	-600	300	ps	12,13,14

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
DQ low impedance time from CK/CK#	tLZ(DQ)	-500	250	-450	225	ps	12,13,14

NOTE 12,13,14: Please refer to page 160, *JEDEC Standard JESD79-3*.

PASS Condition

The measured time interval from the point where the DQ starts to transit from high impedance to the moment when it starts to drive high/low (high impedance state to high/low state), to the clock signal crossing point, should be within the specification limit.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
6. Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.
7. If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.
8. Search for the DQS preamble towards the left from the point where the Read cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.

9 Once the preamble is located, call the “BinaryEdgeNormal” function, using the Clock as the reference to define the Histogram Window for the DQ signal.

10 The Histogram Window is required to cover the DQ signal from the tristate to the moment it starts to drive high/low state.

11 Setup the threshold value and measurement point for the DQ signal based on the histogram result.

12 Once all the points are obtained, proceed with the trigonometry calculation to find the point where the DQ starts to transit from tristate to the time when it start to drive the signal high/low.

13 Assign marker A for the clock signal crossing point while marker B for the data signal start to drive.

14 Measure delta of marker A and marker B and this will be the test result.

15 Compare the test result against the compliance test limit.

Test References

See Table 66 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79-3*.

tDQSQ, DQS-DQ Skew for DQS and Associated DQ Signals - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data strobe output (DQS rising and falling edge) access time to the associated data (DQ rising and falling) signal is within the conformance limit as specified in the *JEDEC Standard JESD79-3*.

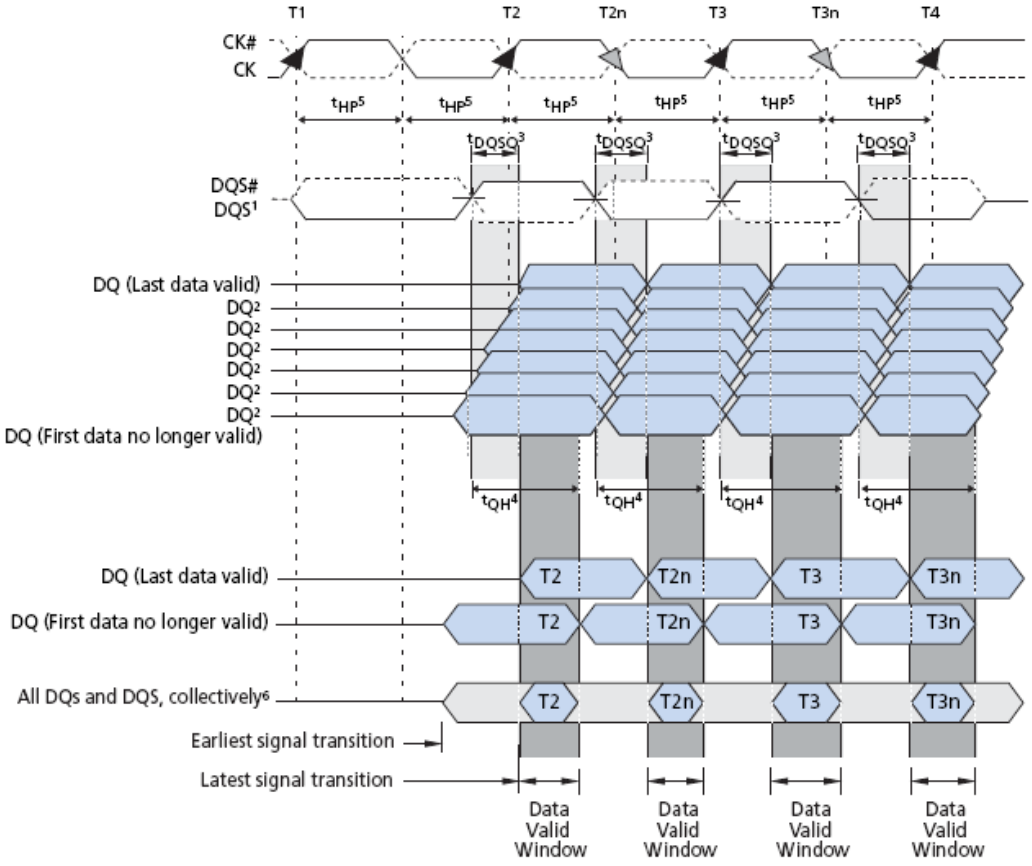


Figure 54 DQS-DQ Skew for DQS and Associated DQ Signals

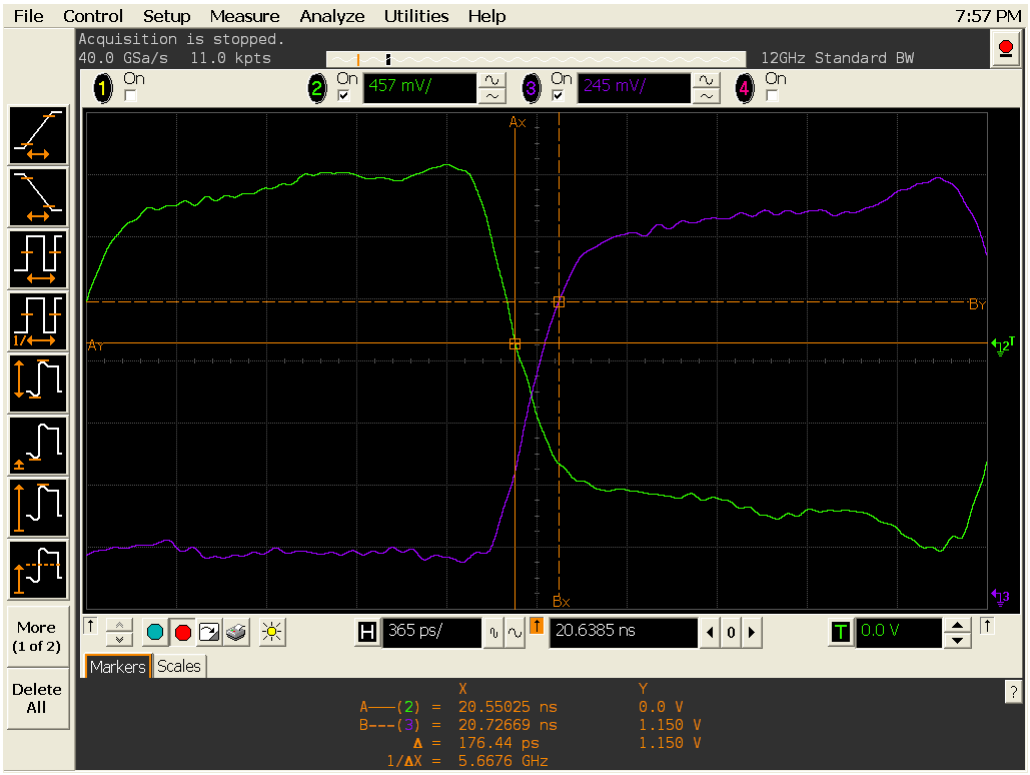


Figure 55 tDQSQ in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Read cycle only):

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 41 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# to DQ skew, per group, per access	tDQSQ	-	200	-	150	ps	12,13

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# to DQ skew, per group, per access	tDQSQ	-	125	-	100	ps	12,13

NOTE 12,13: Please refer to page 160, *JEDEC Standard JESD79-3*.

PASS Condition

The measured time interval between the data strobe and the associated data signal should be within specification limit.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
6. Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.
7. If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.
8. Search for the DQS preamble towards the left from the point where the Read Cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.

9 Once the preamble is located, call the “BinaryEdgeNormal” function to obtain the Edge number of the DQS and DQ signal. This Edge number will be used for the TEdge measurement, in order to locate the points of interest on specific signal.

10 After obtaining the Edge number for the respective signal, begin the tDQSQ measurement bit by bit in the Read data burst, beginning from the 1st bit of the Read cycle.

11 Begin at the 1st bit of the Read cycle, from the Read preamble. Continue the measurement until the last bit (for example, until a tristate happens, which indicates the end of a data burst for the respective Read cycle).

12 DQS-Clock timing measurement compares the rising edge (Vih_ac OR Vil_dc against DQS crossing) OR the falling edge (Vih_ac OR Vil_dc against DQS crossing).

13 Within the data burst, measure each bit, for instance the rising and falling edge of the DQS-Clock. Capture the worst case data each time a new value is measured.

14 Once all bits are validated, assign marker A for the clock signal while marker B for the data signal, for the worst case bit.

15 Measure delta of marker A and marker B and this will be the test result.

16 Compare the test result against the compliance test limit.

Test References

See Table 66 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79-3*.

tQH, DQ/DQS Output Hold Time From DQS - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data output hold time (DQS rising and falling edge) from the DQS (rising and falling edge) is within the conformance limit as specified in the *JEDEC Standard JESD79-3*.

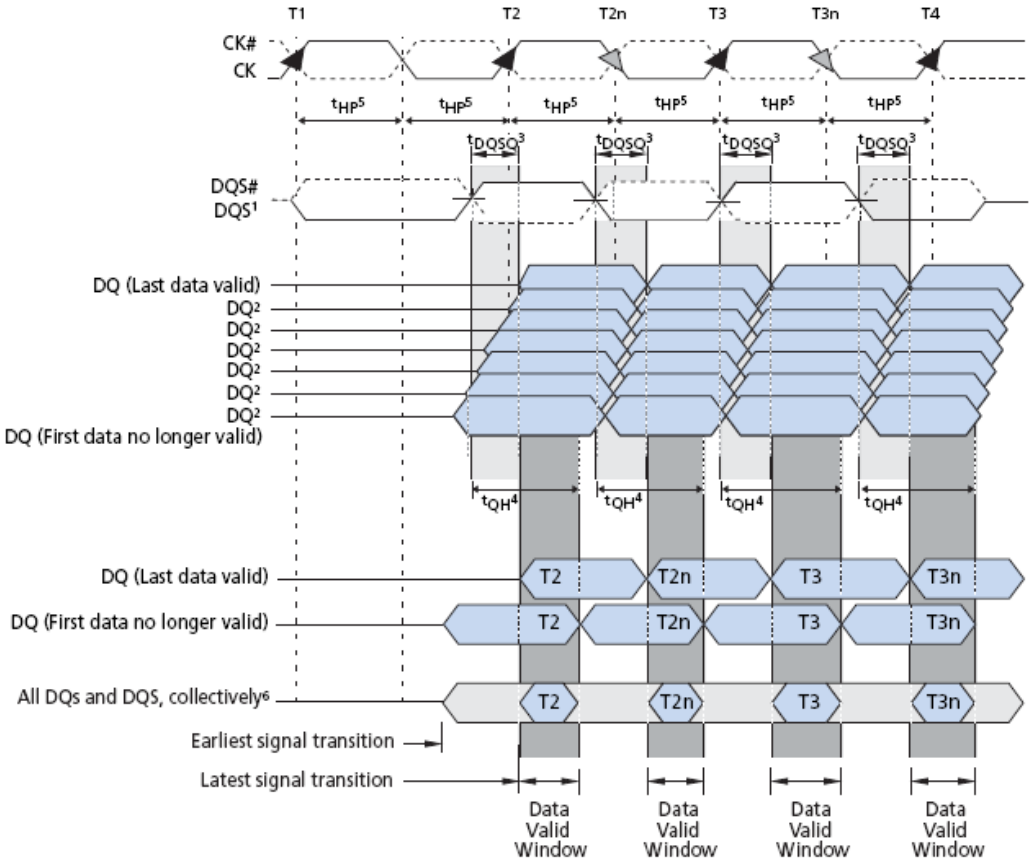


Figure 56 DQ/DQS Output Hold Time From DQS

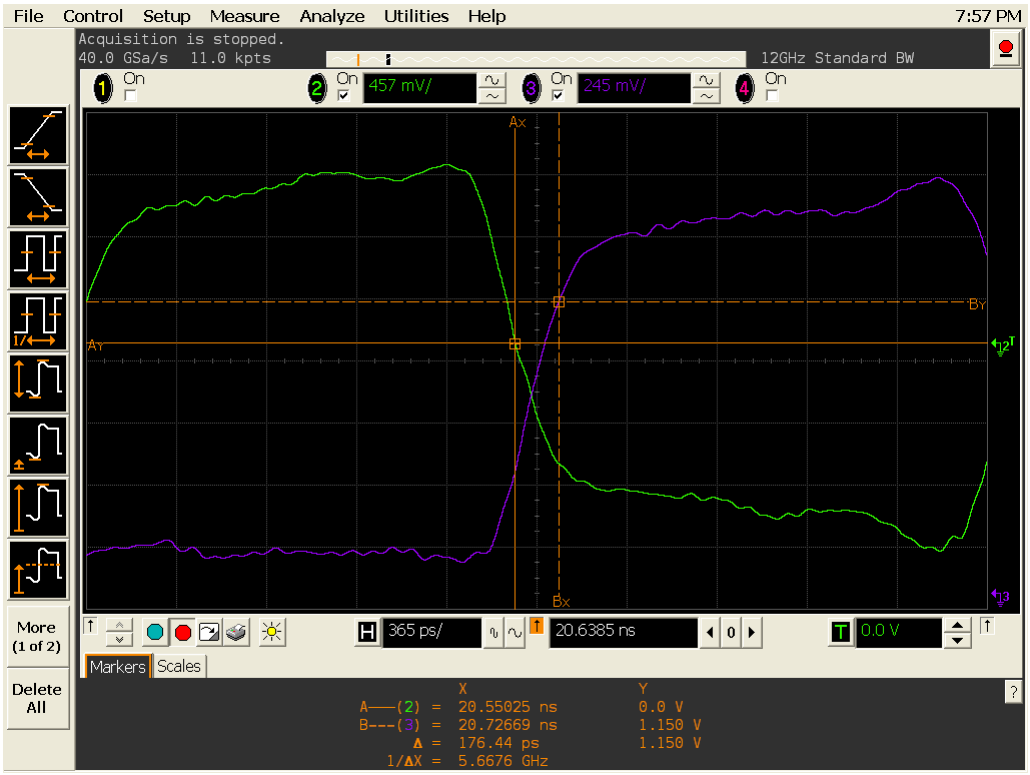


Figure 57 tQH in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Read cycle only):

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 42 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
DQ output hold time from DQS, DQS#	tQH	0.36	-	0.36	-	tCK(avg)	12,13

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
DQ output hold time from DQS, DQS#	tQH	0.36	-	0.36	-	tCK(avg)	12,13

NOTE 12,13: Please refer to page 160, *JEDEC Standard JESD79-3*.

PASS Condition

The measured time interval between the data output hold time and the associated data strobe signal should be within specification limit.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
6. Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.
7. If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.
8. Search for the DQS preamble towards the left from the point where the Read cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.
9. Once the preamble is located, call the “BinaryEdgeNormal” function to obtain the Edge number of the DQS and DQ signal. This Edge number

will be used for the TEdge measurement, in order to locate the points of interest on specific signal.

10 After obtaining the Edge number for the respective signal, begin the tQH measurement bit by bit in Read Data Burst, beginning from the 1st bit of the Read cycle.

11 Begin at the 1st bit of the Read cycle, from the Read preamble. Continue the measurement until the last bit (for instance, until a tristate happens, which indicates the end of a data burst for the respective Read cycle).

12 DQS-DQ timing measurement compares the rising edge (DQS crossing against Vil_dc of the DQ signal, for instance, end of valid DQ hold time) OR the falling edge (DQS crossing against Vih_dc of the DQ signal, for instance, end of valid DQ hold time).

13 Within the data burst, measure each bit, for instance the rising and falling edge of the DQS-DQ. Capture the worst case data each time a new value is measured.

14 Once all bits are validated, assign marker A for the lock signal while marker B for the data signal, for the Worst Case bit.

15 Measure delta of marker A and marker B and this will be the test result.

16 Compare the test result against the compliance test limit.

Test References

See Table 66 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79-3*.

tDQSS, DQS Latching Transition to Associated Clock Edge - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data strobe output (DQS falling edge) access time to the associated clock (crossing point) is within the conformance limit as specified in the *JEDEC Standard JESD79-3*.

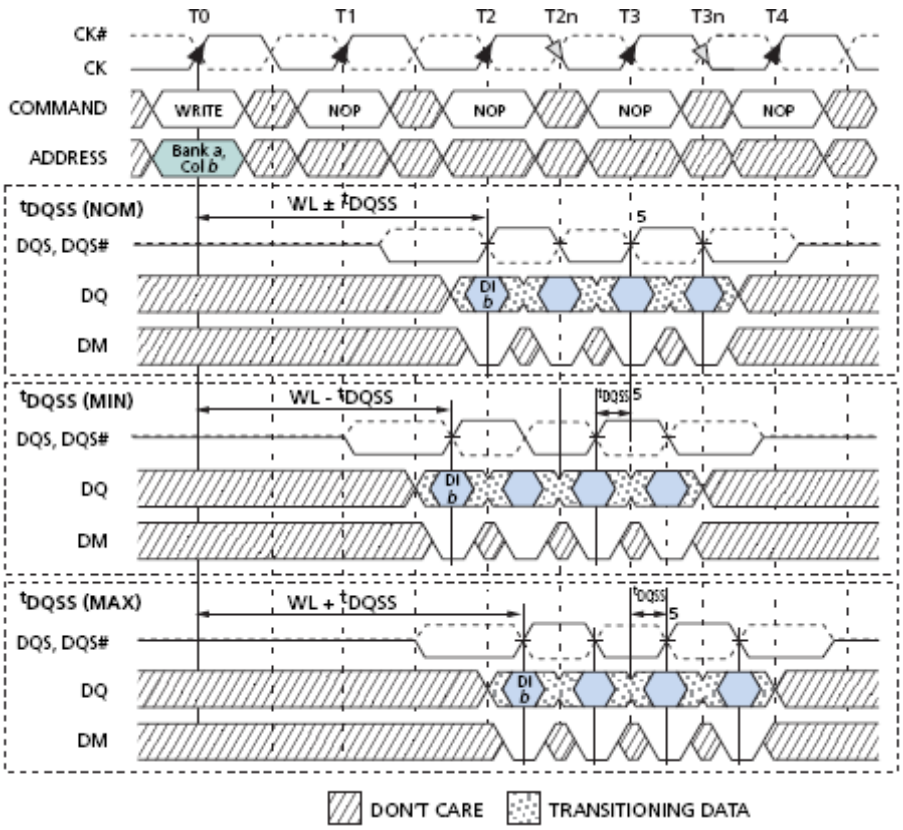


Figure 58 DQS Latching Transition to Associated Clock Edge

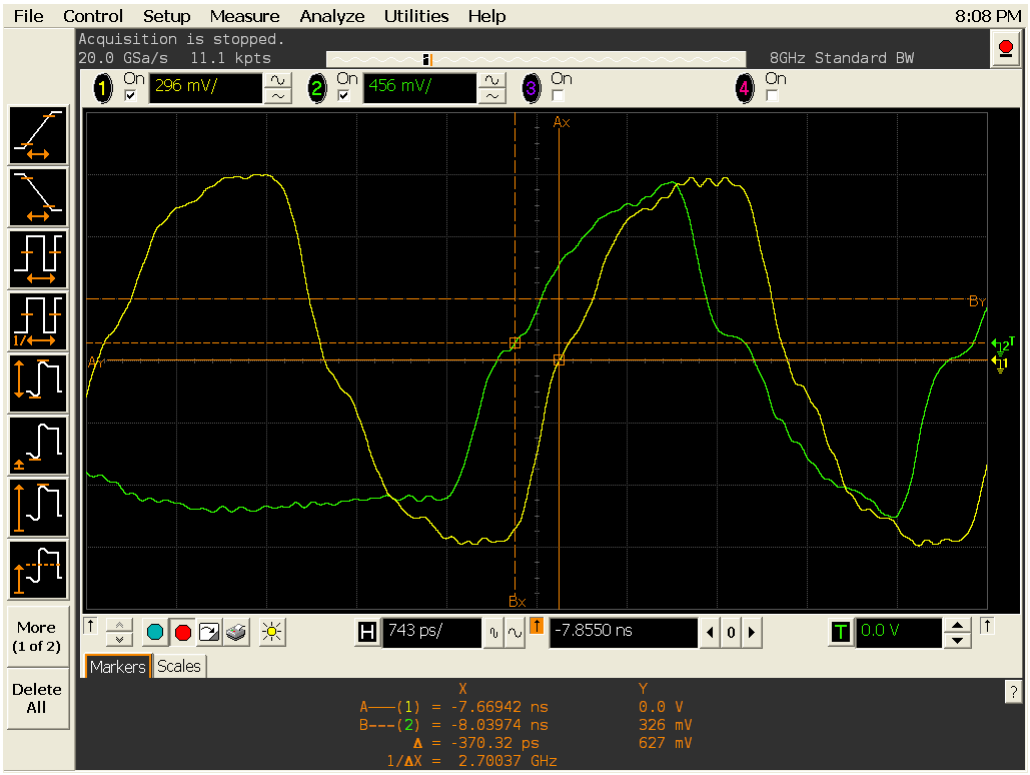


Figure 59 tDQSS in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Write cycle only):

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires additional channel)

Test Definition Notes from the Specification

Table 43 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# rising edge to CHK/CK# rising edge	tDQSS	-0.25	0.25	-0.25	0.25	tCK(avg)	c

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# rising edge to CHK/CK# rising edge	tDQSS	-0.25	0.25	-0.25	0.25	tCK(avg)	c

NOTE c: Please refer to page 160, *JEDEC Standard JESD79-3*.

PASS Condition

The measured time interval between the rising edge of the data strobe access output and the clock crossing should be within specification limit.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
6. Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.
7. If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.
8. Search for the DQS preamble towards the left from the point where the Read cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.

9 Once the preamble is located, call the “BinaryEdgeNormal” function to obtain the Edge number of clock rising edge and strobe rising edge. This Edge number will be used for TEdge measurement, in order to locate the points of interest on specific signal.

10 After obtaining the Edge number for the respective signal, begin the tDQSS measurement bit by bit in the Write data burst, beginning from the 1st bit of the Write cycle. Begin at the 1st bit of the read cycle, from the Write preamble.

11 Continue the measurement until the last bit (for instance, until a tristate happens, which indicates the end of a data burst for the respective Write cycle).

12 DQS-Clock timing measurement compares the rising edge (DQS crossing against clock crossing) OR the falling edge (DQS crossing against Vih_dc of the DQ signal, for instance, end of valid DQ hold time).

13 Within the data burst, measure each bit, for instance the rising edge of the DQS-Clock. Capture the worst case data each time a new value is measured.

14 Once all bits are validated, assign marker A for the clock signal while marker B for the data signal, for the worst case bit.

15 Measure delta of marker A and marker B and this will be the test result.

16 Compare the test result against the compliance test limit.

Test References

See Table 66 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79-3*.

tDQSH, DQS Input High Pulse Width - Test Method of Implementation

The purpose of this test is to verify that the width of the high level of the data strobe signal is within the conformance limit as specified in the *JEDEC Standard JESD79-3*.

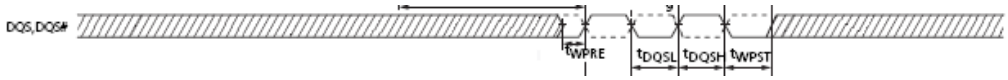


Figure 60 DQS Input High Pulse Width

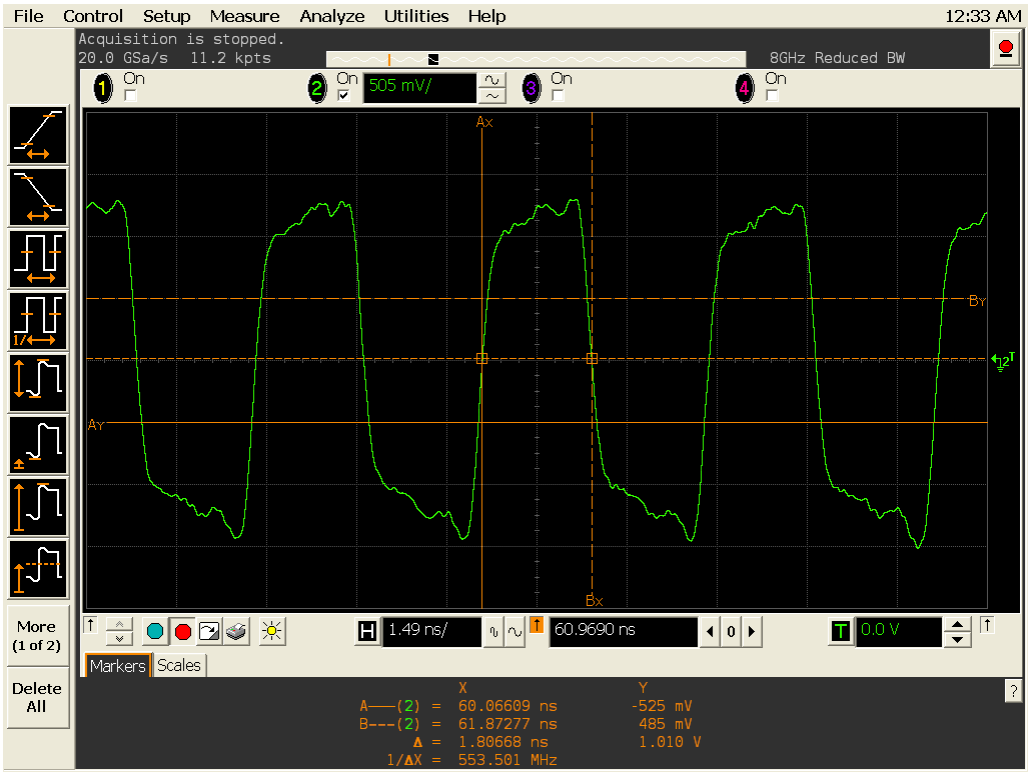


Figure 61 tDQSH in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Read cycle only):

- Data Strobe Signal (DQS as Pin Under Test Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)

- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires additional channel)

Test Definition Notes from the Specification

Table 44 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# differential input high pulse width	tDQSH	0.4	0.6	0.4	0.6	tCK(avg)	

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# differential input high pulse width	tDQSH	0.4	0.6	0.4	0.6	tCK(avg)	

PASS Condition

The measured pwidth of the data strobe signal should be within specification limit.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
4. Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.
5. If you have selected the $\overline{CS}$ option, skip the next step and go to step 7.
6. Search for the DQS preamble towards the left from the point where the Read cycle was previously captured. The for loops, TEdge and Delta Time are used to search the preamble.

7 Once the preamble is located, call the “BinaryEdgeNormal” function to obtain the Edge number. This Edge number will be used to locate the point of interest on the specific signal.

8 After obtaining the Edge number for the respective signal, begin the tDQSH measurement by using the Pwidth function to find any rising edge of the data strobe signal and measure the pwidth for every single bit in the captured data burst.

9 Assign marker A for the rising edge of the clock signal while marker B for the falling edge of the clock signal.

10 Measure delta of marker A and marker B and this will be the test result.

11 Compare the test result against the compliance test limit.

Test References

See Table 66 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79-3*.

tDQSL, DQS Input Low Pulse Width - Test Method of Implementation

The purpose of this test is to verify that the width of the low level of the clock signal is within the conformance limit as specified in the *JEDEC Standard JESD79-3*.

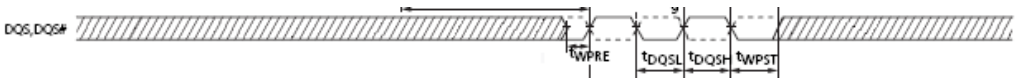


Figure 62 DQS Input Low Pulse Width

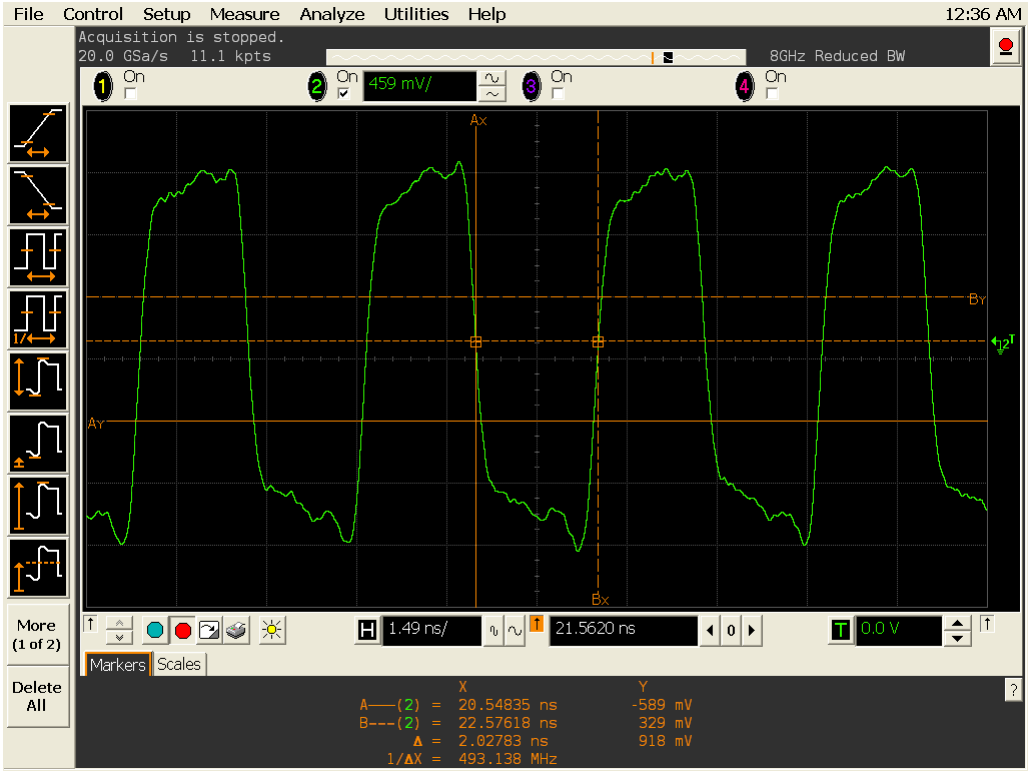


Figure 63 tDQSL in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Read cycle only):

- Data Strobe Signal (DQS as Pin Under Test Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)

- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 45 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# differential input low pulse width	tDQSL	0.4	0.6	0.4	0.6	tCK(avg)	

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# differential input low pulse width	tDQSL	0.4	0.6	0.4	0.6	tCK(avg)	

PASS Condition

The measured nwidth of the clock signal should be within specification limit.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
6. Use the InfiniiScan feature with Setup time and Hold time to find and capture the Read cycle.
7. If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.

8 Search for the DQS preamble towards the left from the point where the Read cycle was previously captured. The for loops, TEdge and Delta Time are used to search the preamble.

9 Once the preamble is located, call the “BinaryEdgeNormal” function to obtain the Edge number. This Edge number will be used to locate the point of interest on the specific signal.

10 After obtaining the Edge number for the respective signal, begin the tDQSL measurement by using the Nwidth function to find any rising edge of the data strobe signal and measure the nwidth for every single bit in the captured data burst.

11 Assign marker A for the rising edge of the clock signal while marker B for the falling edge of the clock signal.

12 Measure delta of marker A and marker B and this will be the test result.

13 Compare the test result against the compliance test limit.

Test References

See Table 66 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79-3*.

tDSS, DQS Falling Edge to CK Setup Time - Test Method of Implementation

The purpose of this test is to verify that the time interval from the falling edge of the data strobe (DQS falling edge) output access time to the clock setup time, is within the conformance limit as specified in the *JEDEC Standard JESD79-3*.

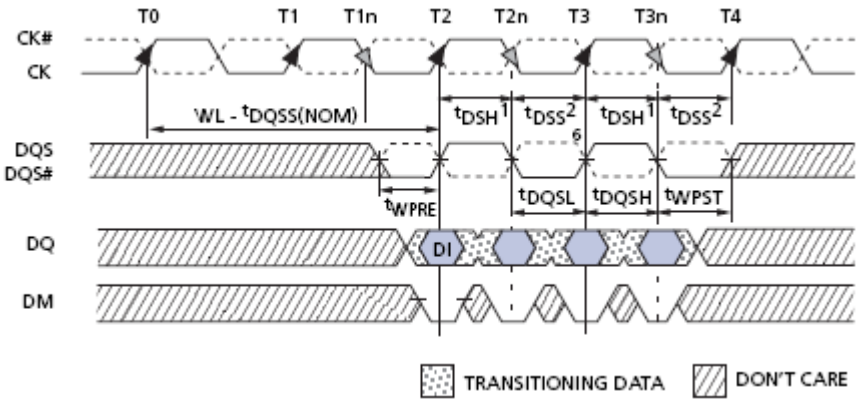


Figure 64 DQS Falling Edge to CK Setup Time

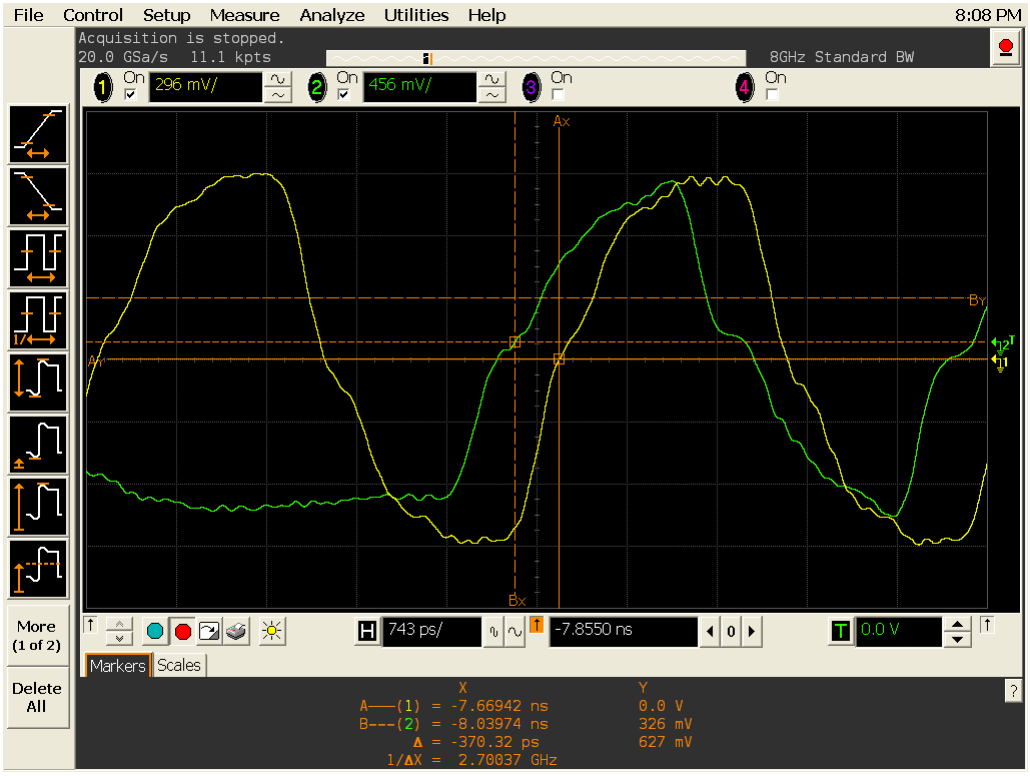


Figure 65 tDSS in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Write cycle only):

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 46 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# falling edge setup time to CK, CK# rising edge	tDSS	0.2	-	0.2	-	tCK(avg)	c

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# falling edge setup time to CK, CK# rising edge	tDSS	0.2	-	0.2	-	tCK(avg)	c

NOTE c: Please refer to page 160, *JEDEC Standard JESD79-3*.

PASS Condition

The measured time interval between the falling edge of the data strobe access output to the associated clock setup time should be within the specification limit.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.

3 Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.

4 Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.

5 Chip Select ($\overline{CS}$) option is only applicable if the user has selected "Yes" for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.

6 Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.

7 If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.

8 Search for the DQS preamble towards the left from the point where the Write cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.

9 Once the preamble is located, call the "BinaryEdgeNormal" function to obtain the Edge number. This Edge number will be used to locate the point of interest on the specific signal.

10 After obtaining the Edge number for the respective signal, begin the tDSS measurement bit by bit in Write data burst.

11 Begin at the 1st bit of the Write cycle, from the Write preamble. Continue the measurement until the last bit (for example, until a tristate happens, which indicates the end of a data burst for the respective Write cycle).

12 DQS-Clock timing measurement compares the rising edge (DQS falling against clock crossing).

13 DQ-Clock timing measurement compares the falling edge of the DQS to the clock setup time. The worst case data will be captured each time new value is measured.

14 Once all bits are validated, assign marker A for the clock signal while marker B for the data signal, for the worst case bit.

15 Measure delta of marker A and marker B and this will be the test result.

16 Compare the test result against the compliance test limit.

Test References

See Table 66 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79-3*.

tDSH, DQS Falling Edge Hold Time from CK - Test Method of Implementation

The purpose of this test is to verify that the time interval from the falling edge of the data strobe output access time to the hold time of the clock, must be within the conformance limit as specified in the *JEDEC Standard JESD79-3*.

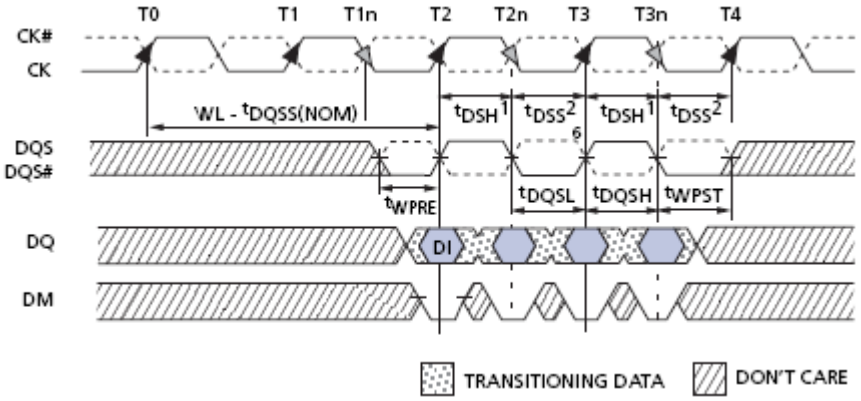


Figure 66 DQS Falling Edge Hold Time

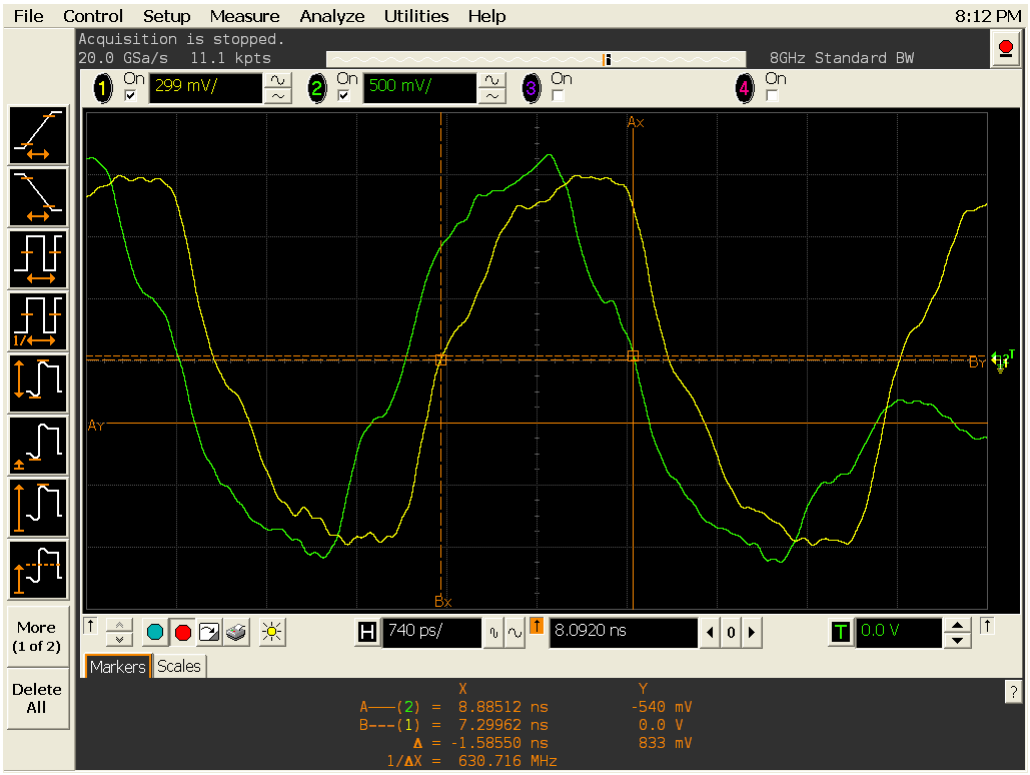


Figure 67 tDSH in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Write cycle only):

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 47 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# falling edge hold time from CK, CK# rising edge	tDSH	0.2	-	0.2	-	tCK(avg)	c

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# falling edge hold time from CK, CK# rising edge	tDSH	0.2	-	0.2	-	tCK(avg)	c

NOTE c: Please refer to page 160, *JEDEC Standard JESD79-3*.

PASS Condition

The measured time interval between the falling edge of the data strobe hold time from the associated clock crossing edge should be within the specification limit.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
6. Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.
7. If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.
8. Search for the DQS preamble towards the left from the point where the Write cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.

9 Once the preamble is located, call the “BinaryEdgeNormal” function to obtain the Edge number. This Edge number will be used to locate the point of interest on the specific signal.

10 After obtaining the Edge number for the respective signal, begin the tDSH measurement bit by bit in Write data burst.

11 Begin at the 1st bit of the Write cycle, from the Write preamble. Continue the measurement until the last bit (for example, until a tristate happens, which indicates the end of a data burst for the respective Write cycle).

12 DQS-Clock timing measurement compares the falling edge of the DQS crossing hold time from the respective clock crossing edge.

13 Within the data burst, each bit, for instance, the falling edge of DQS-Clock will be measured. The worst case data will be captured each time a new value is measured.

14 Once all the bits are validated, assign marker A for the clock signal while marker B for the data signal, for the worst case bit.

15 Measure delta of marker A and marker B and this will be the test result.

16 Compare the test result against the compliance test limit.

Test References

See Table 66 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79-3*.

tWPST, Write Postamble - Test Method of Implementation

The purpose of this test is to verify that the time when the DQS is no longer driving (from high/low state to high impedance) from the last DQS signal crossing (last bit of the write data burst) for the Write cycle, is within the conformance limit as specified in the *JEDEC Standard JESD79-3*.

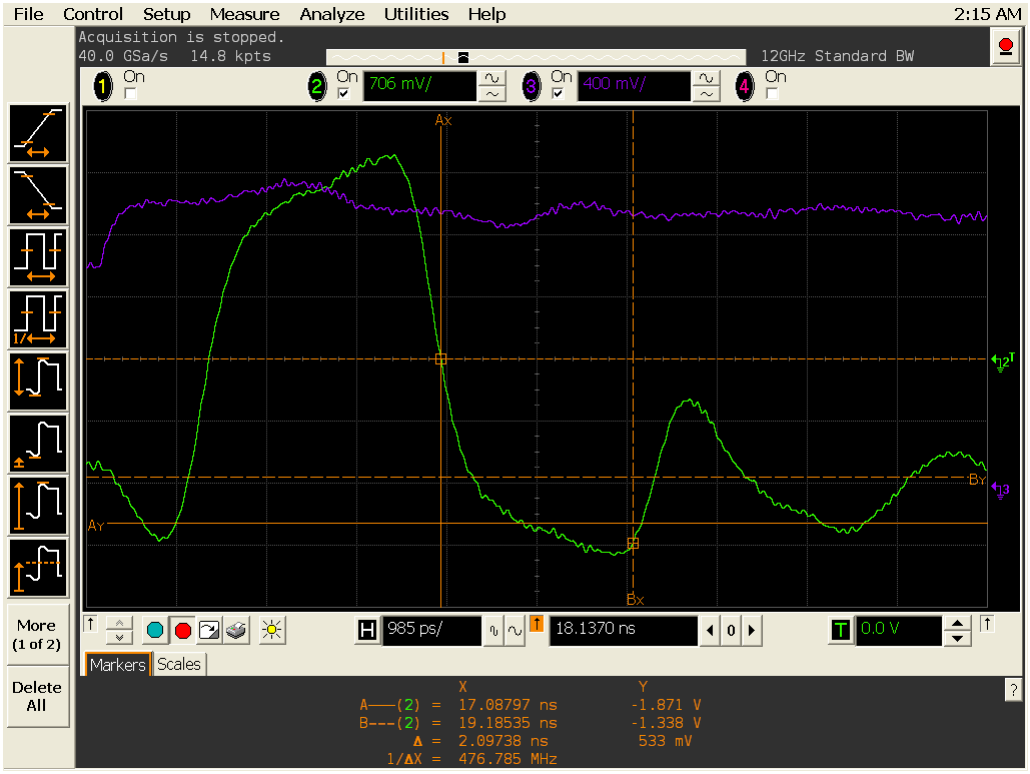


Figure 68 tWPST in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Write cycle only):

- Data Strobe Signal (DQS as Pin Under Test Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 48 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# differential WRITE Postamble	tWPST	0.4	-	0.4	-	tCK(avg)	1

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# differential WRITE Postamble	tWPST	0.4	-	0.4	-	tCK(avg)	1

NOTE 1: Please refer to page 160, *JEDEC Standard JESD79-3*.

PASS Condition

The measured time interval between the last DQS signal crossing point and the point where the DQS starts to transit from high/low state to high impedance should be within the specification limit.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
6. Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.
7. If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.

8 Search for the DQS postamble towards the right from the point where the Write cycle was previously captured. The For loops, TEdge and Delta Time are used to search the postamble.

9 Once the postamble is located, call the “BinarySearchNormal” function to locate the last DQS crossing point or reference point.

10 Define the histogram window in order to obtain the Min and Max voltage for the DQS postamble signal and it will be used for the threshold setup for the trigonometry calculation later.

11 Once all points are obtained, proceed with the trigonometry calculation to find the point where the DQS starts to transit from high/low to the time when it starts to turn off the driver low (for instance, end of burst or postamble).

12 Assign marker A for the DQS signal crossing point while marker B for the data strobe signal start to turn off driver.

13 Measure delta of marker A and marker B and this will be the test result.

14 Compare the test result against the compliance test limit.

Test References

See Table 66 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79-3*.

tWPRE, Write Preamble - Test Method of Implementation

The purpose of this test is to verify that the time when the DQS starts to drive low (preamble behavior) to the first DQS signal crossing for the Write cycle, is within the conformance limit as specified in the *JEDEC Standard JESD79-3*.

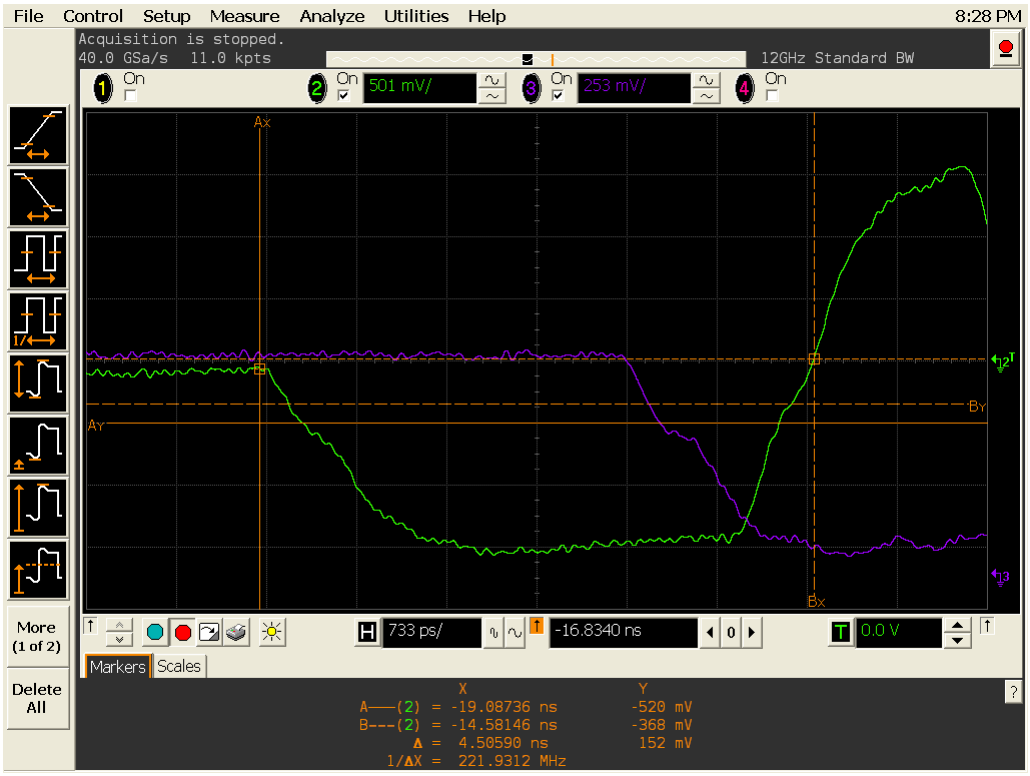


Figure 69 tWPRE in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Write cycle only):

- Data Strobe Signal (DQS as Pin Under Test Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 49 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# differential WRITE Preamble	tWPRE	0.9	-	0.9	-	tCK(avg)	1

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# differential WRITE Preamble	tWPRE	0.9	-	0.9	-	tCK(avg)	1

NOTE 1: Please refer to page 160, *JEDEC Standard JESD79-3*.

PASS Condition

The measured time interval of the point where the DQS starts to transit from tristate (high impedance state to low state) to the DQS signal crossing point for the Write cycle, should be within the specification limit.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
6. Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.
7. If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.
8. Search for the DQS preamble towards the left from the point where the Write cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.

9 Once the preamble is located, call the “BinarySearchNormal” function to locate the first DQS crossing point or the reference point.

10 Define the histogram window in order to obtain the Min and Max voltage for the DQS preamble signal and it will be used for the threshold setup for the trigonometry calculation later.

11 Once all the points are obtained, proceed with the trigonometry calculation to find the point where the DQS starts to transit from tristate to the time when it starts to drive low (for instance, beginning of preamble).

12 Assign marker A for the DQS signal crossing point while marker B for the data strobe signal start to drive low.

13 Measure delta of marker A and marker B and this will be the test result.

14 Compare the test result against the compliance test limit.

Test References

See Table 66 - Timing Parameters by Bin, in the *JEDEC Standard JESD79-3*.

tRPRE, Read Preamble - Test Method of Implementation

The purpose of this test is to verify that the time when the DQS start driving low (*preamble behavior) to the first DQS signal crossing for the Read cycle must be within the conformance limit as specified in the *JEDEC Standard JESD79-3*.

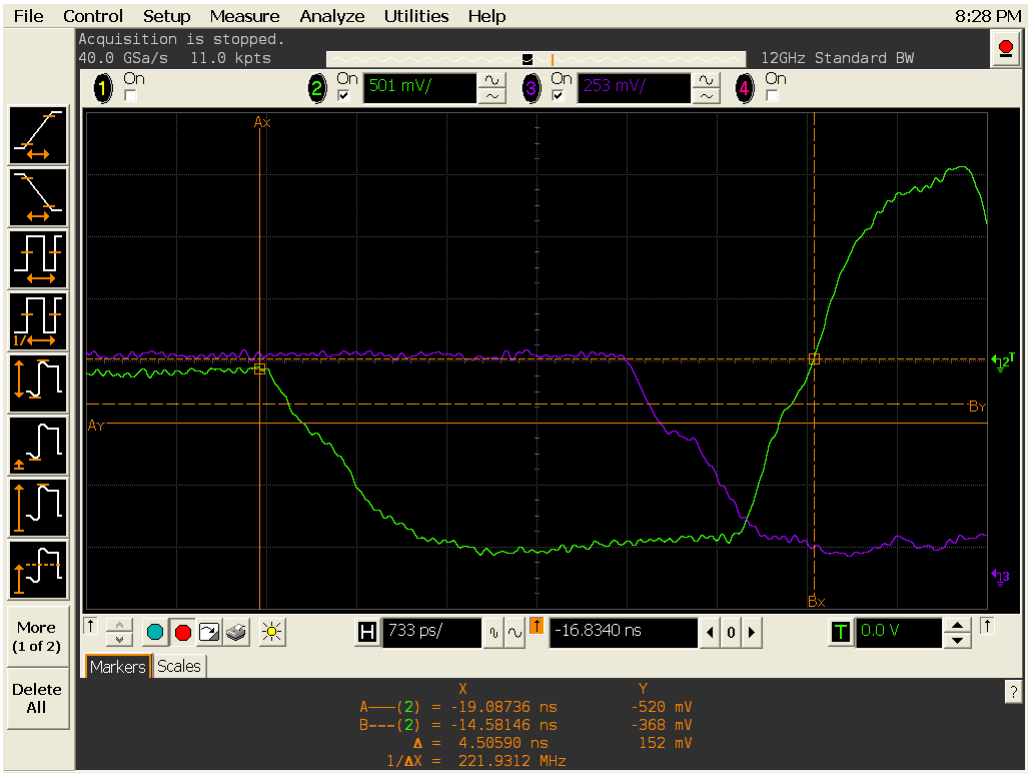


Figure 70 tRPRE in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Read cycle only):

- Data Strobe Signal (DQS as Pin Under Test Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires additional channel)

Test Definition Notes from the Specification

Table 50 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# differential READ Preamble	tRPRE	0.9	Note 19	0.9	Note 19	tCK(avg)	1,19

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# differential READ Preamble	tRPRE	0.9	Note 19	0.9	Note 19	tCK(avg)	1,19

NOTE 1,19: Please refer to page 160, *JEDEC Standard JESD79-3*.

PASS Condition

The measured time interval of the point where the DQS starts to transit from tristate (high impedance state to low state) to the DQS signal crossing point for the Read cycle should be within the specification limit.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
6. Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.
7. If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.
8. Search for the DQS preamble towards the left from the point where the Read cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.

9 Once the preamble is located, call the “BinarySearchNormal” function to locate the first DQS crossing point or the reference point.

10 Define the histogram window in order to obtain the Min and Max voltage for the DQS preamble signal and it will be used for the threshold setup for the trigonometry calculation later.

11 Once all the points are obtained, proceed with the trigonometry calculation to find the point where the DQS starts to transit from tristate to the time when it start to drive low (for instance, beginning of preamble).

12 Assign marker A for the DQS signal crossing point while marker B for the data strobe signal start to drive low.

13 Measure delta of marker A and marker B and this will be the test result.

14 Compare the test result against the compliance test limit.

Test References

See Table 66 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79-3*.

tRPST, Read Postamble - Test Method of Implementation

The purpose of this test is to verify that the time when the DQS is no longer driving (from high/low state to high-impedance) to the last DQS signal crossing (last bit of the data burst) for the Read cycle is within the conformance limit as specified in the *JEDEC Standard JESD79-3*.

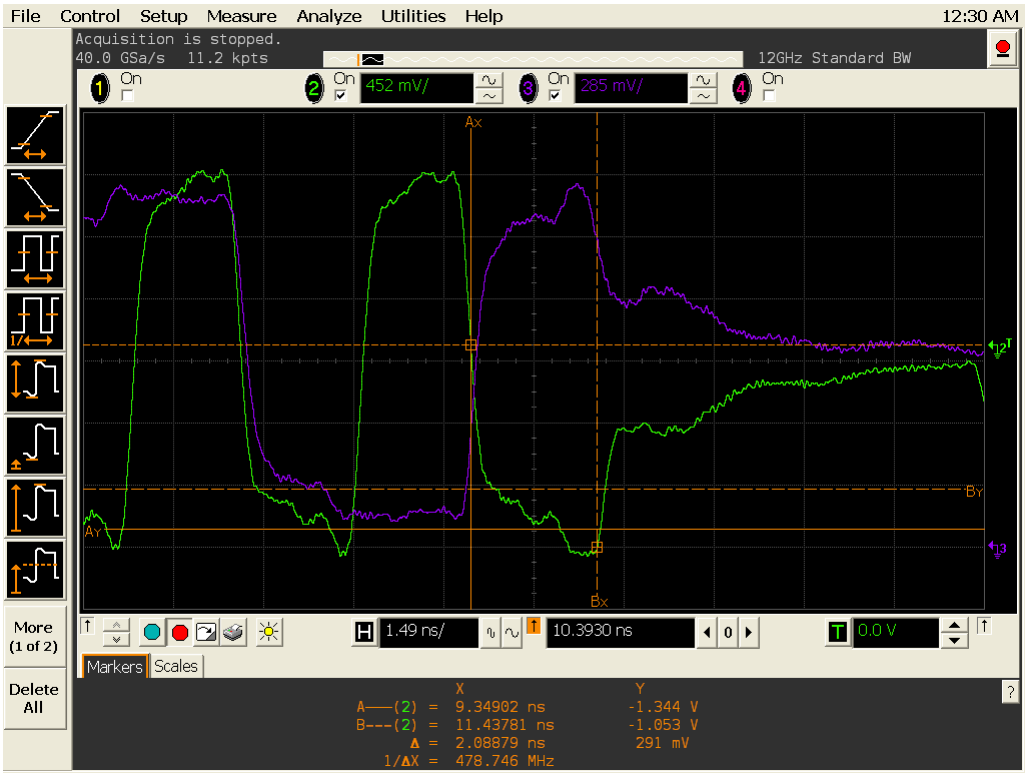


Figure 71 tRPST in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Read cycle only):

- Data Strobe Signal (DQS as Pin Under Test Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 51 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# differential READ Postamble	tRPST	0.3	Note 11	0.3	Note 11	tCK(avg)	11, 12,13

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# differential READ Postamble	tRPST	0.3	Note 11	0.3	Note 11	tCK(avg)	11, 12,13

NOTE 11, 12,13: Please refer to page 160, *JEDEC Standard JESD79-3*.

PASS Condition

The measured time interval between the last DQS signal crossing point to the point where the DQS starts to transit from high/low level to high impedance for the Read cycle should be within the specification limit.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope setting. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
6. Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.
7. If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.

8 Search for the DQS postamble towards the right from the point where the Read cycle was previously captured. The For loops, TEdge and Delta Time are used to search the postamble.

9 Once the postamble is located, call the “BinarySearchNormal” function to locate the last DQS crossing point or reference point.

10 Define the histogram window in order to obtain the Min and Max voltage for the DQS postamble signal and it will be used for the threshold setup for the trigonometry calculation later.

11 Once all points are obtained, proceed with the trigonometry calculation to find the point where the DQS starts to transit from high/low to the time when it starts to turn off the driver low (for instance, end of burst, postamble).

12 Assign marker A for the DQS signal crossing point while marker B for the data strobe signal start to turn off the driver.

13 Measure delta of marker A and marker B and this will be the test result.

14 Compare the test result against the compliance test limit.

Test References

See Table 66 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79-3*.

11 Data Mask Timing (DMT) Tests

This section provides the Methods of Implementation (MOIs) for Data Mask Timing tests using an Agilent 54850A series or 80000 series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR3 Compliance Test Application.

NOTE Both XYZ# and $\overline{\text{XYZ}}$ are referring to compliment. Thus, CK# is the same as $\overline{\text{CK}}$.

Probing for Data Mask Timing Tests

When performing the Data Mask Timing tests, the DDR3 Compliance Test Application will prompt you to make the proper connections. The connection for Data Mask Timing tests may look similar to the following diagrams. Refer to the Connection tab in DDR3 Electrical Performance Compliance Test application for the exact number of probe connections. Typically, you need minimum three probe connections to run the tests.

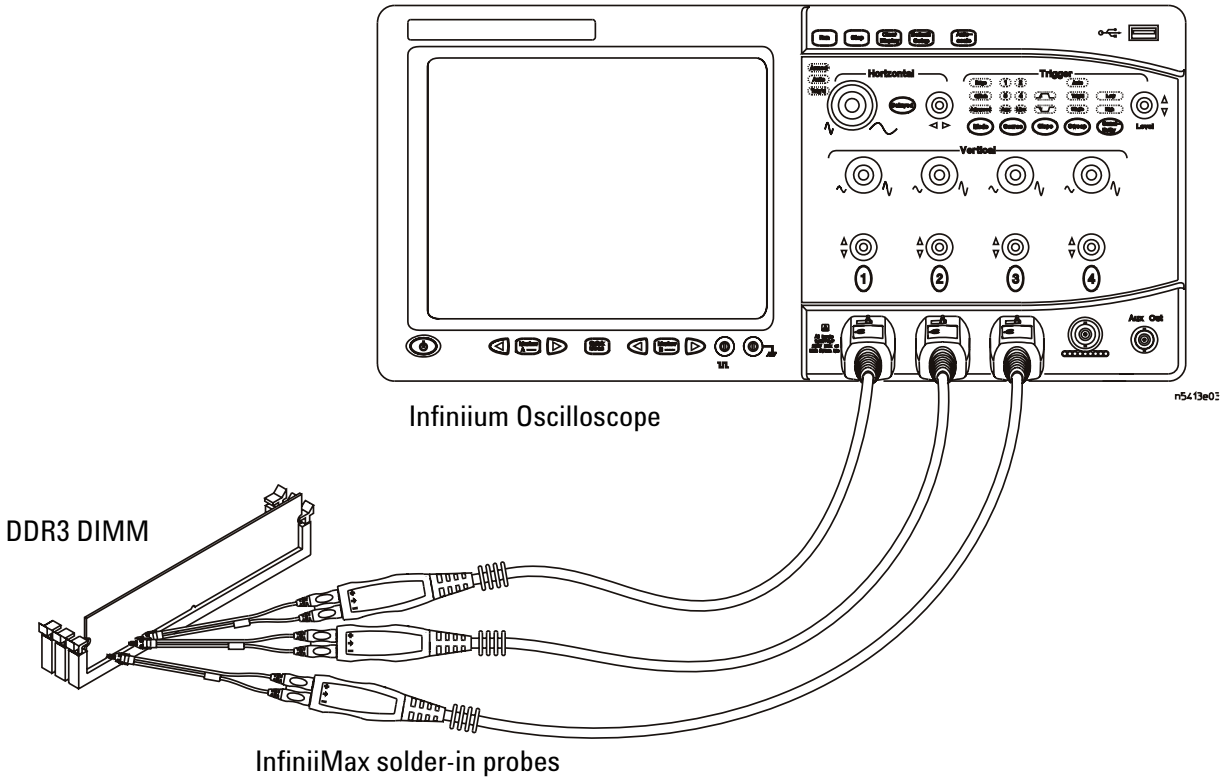


Figure 72 Probing for Data Mask Timing Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR3 Compliance Test Application. (The channels shown in Figure 72 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 16, “InfiniiMax Probing,” starting on page 261.

Test Procedure

1. Start the automated test application as described in “Starting the DDR3 Compliance Test Application" on page 27.
2. Ensure that the RAM reliability test software is running on the computer system where the DDR3 Device Under Test (DUT) is attached. This software will perform test on all the unused RAM on the system by producing repetitive burst of read-write data signals to the DDR3 memory.
3. Connect the differential solder-in probe head to the PUTs on the DDR3 DIMM.
4. Connect the oscilloscope probes to any channels of the oscilloscope.
5. In the DDR3 Test application, click the Set Up tab.
6. Select the Speed Grade options. For Data Mask Timing Tests, you can select any speed grade within the selection: DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600.
7. Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.
8. Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

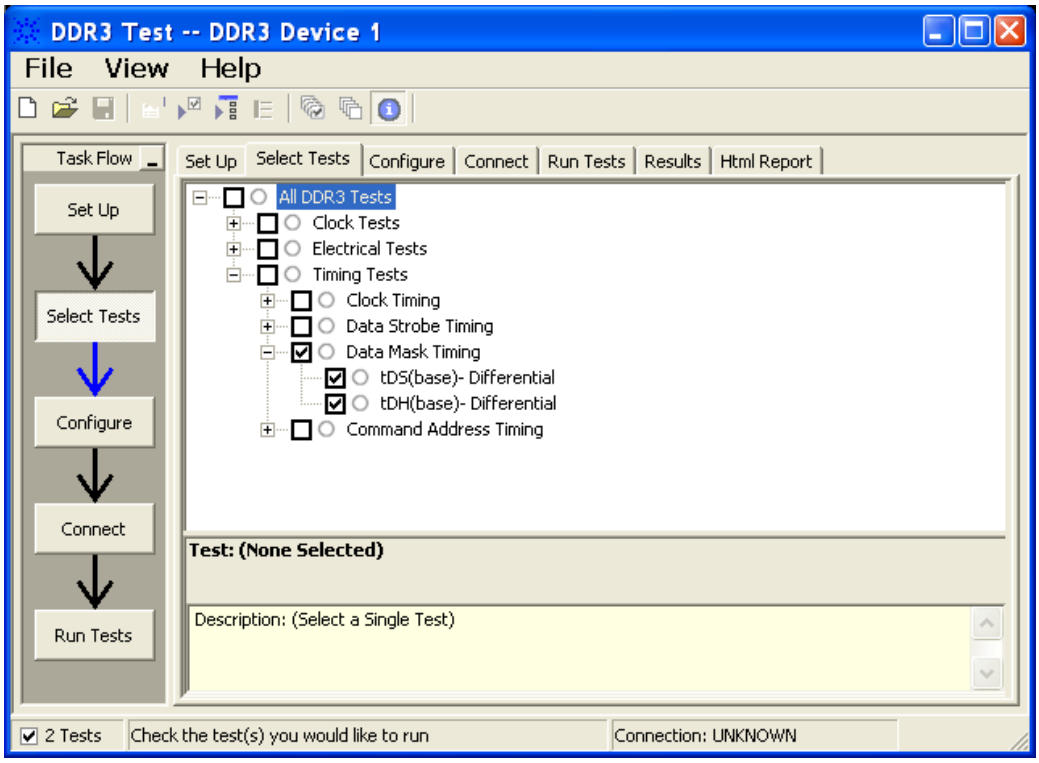


Figure 73 Selecting Data Mask Timing Tests

9 Follow the DDR3 Test application's task flow to set up the configuration options (see Table 52), run the tests and view the tests results.

Table 52 Test Configuration Options

Configuration Option	Description
Stop on error	Enabling this option will allow error messages to prompt whenever the test criteria is not met. Disabling this option will allow the system to bypass all the error messages that could occur and proceed to the next test. This option is suitable for long hours multiple trials.
Signal Threshold setting by percentage	This option allows you to define the Upper and Lower threshold of the signal by percentage.
VDD	Input supply voltage value.
VDDQ	Input supply voltage for data output.
Vref	Input reference voltage value.
Vih(DC)	Input voltage high value (direct current).
Vih(AC)	Input voltage high value (alternating current).
Vil(DC)	Input voltage low value (direct current).
Vil(AC)	Input voltage low value (alternating current).
Timing Tests	
Total Bit Display	Allows you to select the number of data bits to be displayed at the end of the test. Selecting more bits gives a better view of the entire burst of signals.
Verify Selected Rank Only?	If you choose Yes, you require an additional channel for the Chip Select (CS). Measurement will only be done on the selected rank based on the Chip Select signal connected to the oscilloscope.
Channel (1,2,3)	Signal connected to the specific channel.
Pin Under Test, PUT	Signal used for testing.

tDS(base), Differential DQ and DM Input Setup Time - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data or data mask (DQ/DM rising/falling Edge) setup time to the associated DQS crossing edge is within the conformance limits as specified in the *JEDEC Standard JESD79-3*.

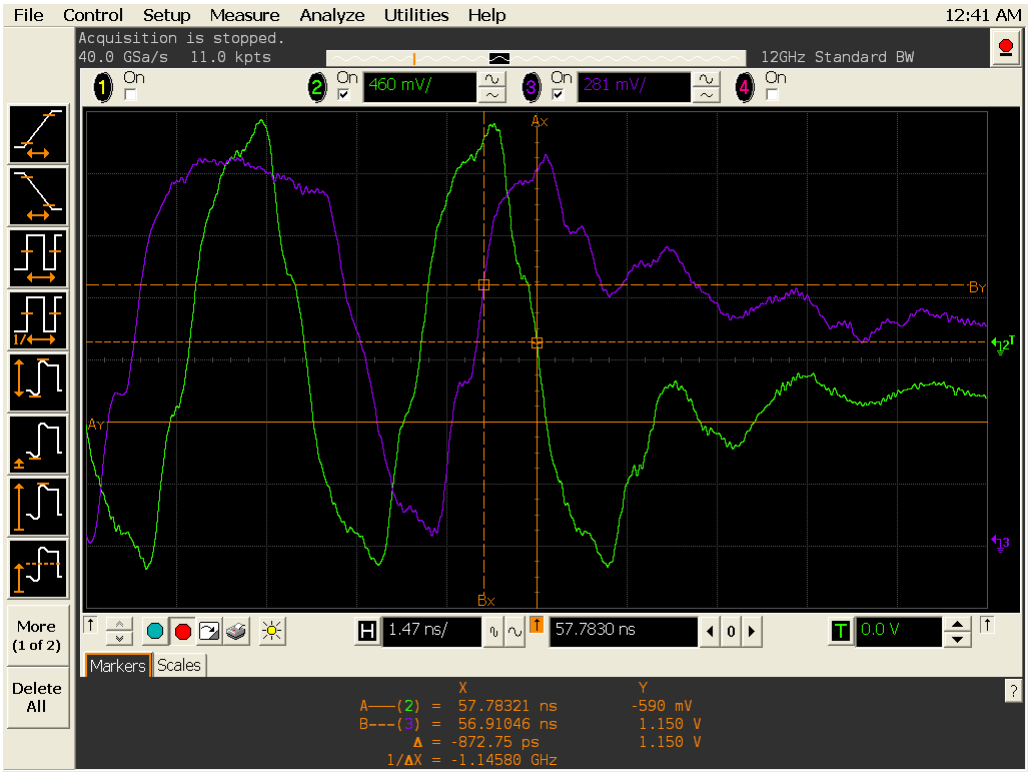


Figure 74 tDS(base) in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal (DQ as Pin Under Test Signal)

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)
  - Use differential connection (DQS+ and DQS-)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires additional channel)

Test Definition Notes from the Specification

Table 53 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
Data setup time to DQS, DQS# referenced to Vih(ac), Vil(ac) levels	tDS(base)	75	-	25	-	ps	d, 17

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
Data setup time to DQS, DQS# referenced to Vih(ac), Vil(ac) levels	tDS(base)	TBD	-	TBD	-	ps	d, 17

NOTE d, 17: Please refer to page 160, *JEDEC Standard JESD79-3*.

PASS Condition

The measured time interval between the data or data mask (DQ/DM) setup time to the respective DQS crossing point should be within the specification limit.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
6. Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.

7 If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.

8 Search for the DQS preamble towards the left from the point where the Write cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.

9 Once the preamble is located, call the “BinaryEdgeNormal” function to obtain the Edge number of the rise/fall DQS crossing and Vih_ac/Vil_ac DQ for later TEdge measurement use. This Edge number will be used to locate the point of interest on the specific signal.

10 After obtaining the Edge number for the respective signal, begin the tDS(base) measurement bit by bit in the Write data burst. Begin at the 1st bit of the Write cycle, from the Write preamble.

11 Continue the measurement until the last bit (for example, until a tristate happens, which indicates the end of a data burst for the respective Write cycle).

12 The DQS-DQ timing measurement compares the rising edge (DQ rising, for instance Vih_ac against associated DQS crossing) OR the falling edge (DQ falling, for instance Vil_ac against associated DQS crossing).

13 Within the data burst, measure each bit, for instance rising and falling edge of DQS-DQ. Capture the worst case data each time a new value is measured.

14 Once all bits are validated, assign marker A for the clock signal while marker B for the data signal, for the worst case bit.

15 Measure delta of marker A and marker B and this will be the test result.

16 Compare the test result against the compliance test limit.

Test References

See Table 66 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79-3*.

tDH(base), Differential DQ and DM Input Hold Time - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data or data mask (DQ/DM rising/falling edge) setup time to the associated DQS crossing edge is within the conformance limits as specified in the *JEDEC Standard JESD79-3*.

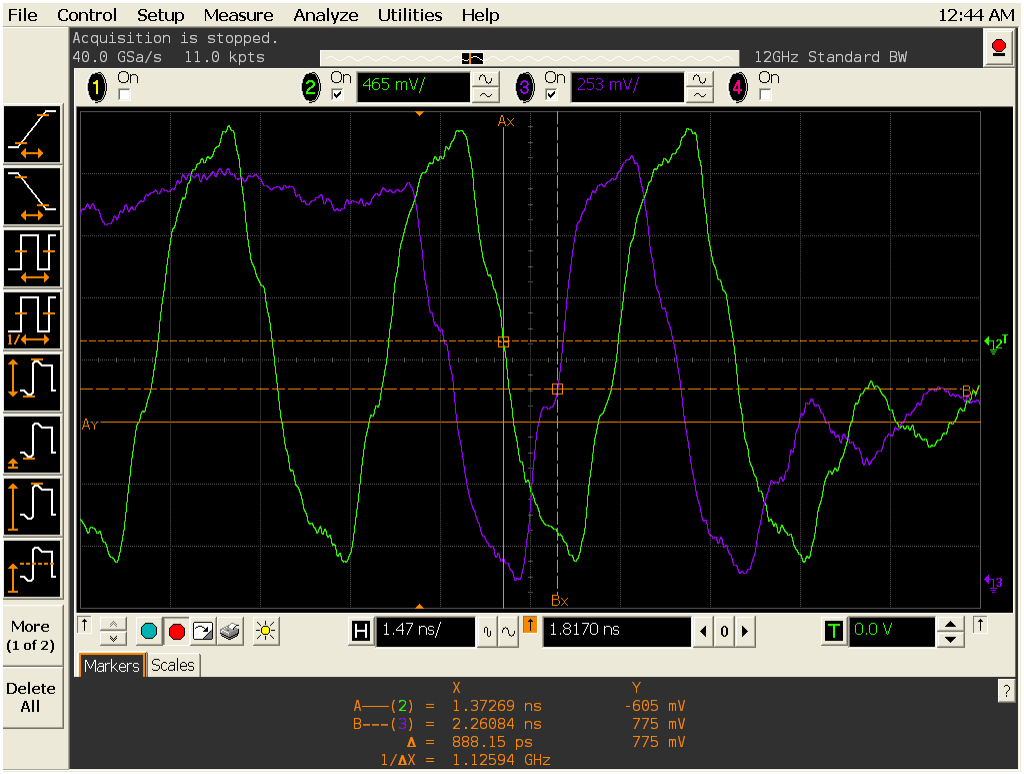


Figure 75 tDH(base) in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal (DQ as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)
  - Use differential connection (DQS+ and DQS-)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 54 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
Data hold time from DQS, DQS# referenced to Vih(ac), Vil(ac) levels	tDH(base)	150	-	100	-	ps	d, 17

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
Data hold time from DQS, DQS# referenced to Vih(ac), Vil(ac) levels	tDH(base)	TBD	-	TBD	-	ps	d, 17

NOTE d, 17: Please refer to page 160, *JEDEC Standard JESD79-3*.

PASS Condition

The measured time interval between the data or data mask (DQ/DM) hold time to the respective DQS crossing point should be within the specification limit.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
6. Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.

7 If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.

8 Search for the DQS preamble towards the left from the point where the Write cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.

9 Once the preamble is located, call the “BinaryEdgeNormal” function to obtain the Edge number of the rise/fall DQS crossing and the Vih_dc/Vil_dc DQ for the later TEdge measurement use. This Edge number will be used to locate the point of interest on the specific signal.

10 After obtaining the Edge number for the respective signal, begin the tDH(base) measurement bit by bit in the Write data burst. Begin at the 1st bit of the Write cycle, from the Write preamble.

11 Continue the measurement until the last bit (for example, until a tristate happens, which indicates the end of a data burst for the respective Write cycle).

12 The DQS-DQ timing measurement compares the rising edge (DQ rising, for instance Vil_dc against associated DQS crossing) OR the falling edge (DQ falling, for instance Vih_dc against associated DQS crossing).

13 Within the data burst, measure each bit, for instance rising and falling edge of the DQS-DQ. Capture the worst case data each time a new value is measured.

14 Once all bits are validated, assign marker A for the clock signal while marker B for the data signal, for the worst case bit.

15 Measure delta of marker A and marker B and this will be the test result.

16 Compare the test result against the compliance test limit.

Test References

See Table 66 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79-3*.

12 Command and Address Timing (CAT) Tests

This section provides the Methods of Implementation (MOIs) for Command and Address Timing tests using an Agilent 54850A series or 80000 series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR3 Compliance Test Application.

NOTE Both XYZ# and $\overline{\text{XYZ}}$ are referring to compliment. Thus, CK# is the same as $\overline{\text{CK}}$.

Probing for Command and Address Timing Tests

When performing the Command and Address Timing tests, the DDR3 Compliance Test Application will prompt you to make the proper connections. The connection for Command and Address Timing tests may look similar to the following diagrams. Refer to the Connection tab in DDR3 Electrical Performance Compliance Test application for the exact number of probe connections. Typically, you need minimum three probe connections to run the tests.

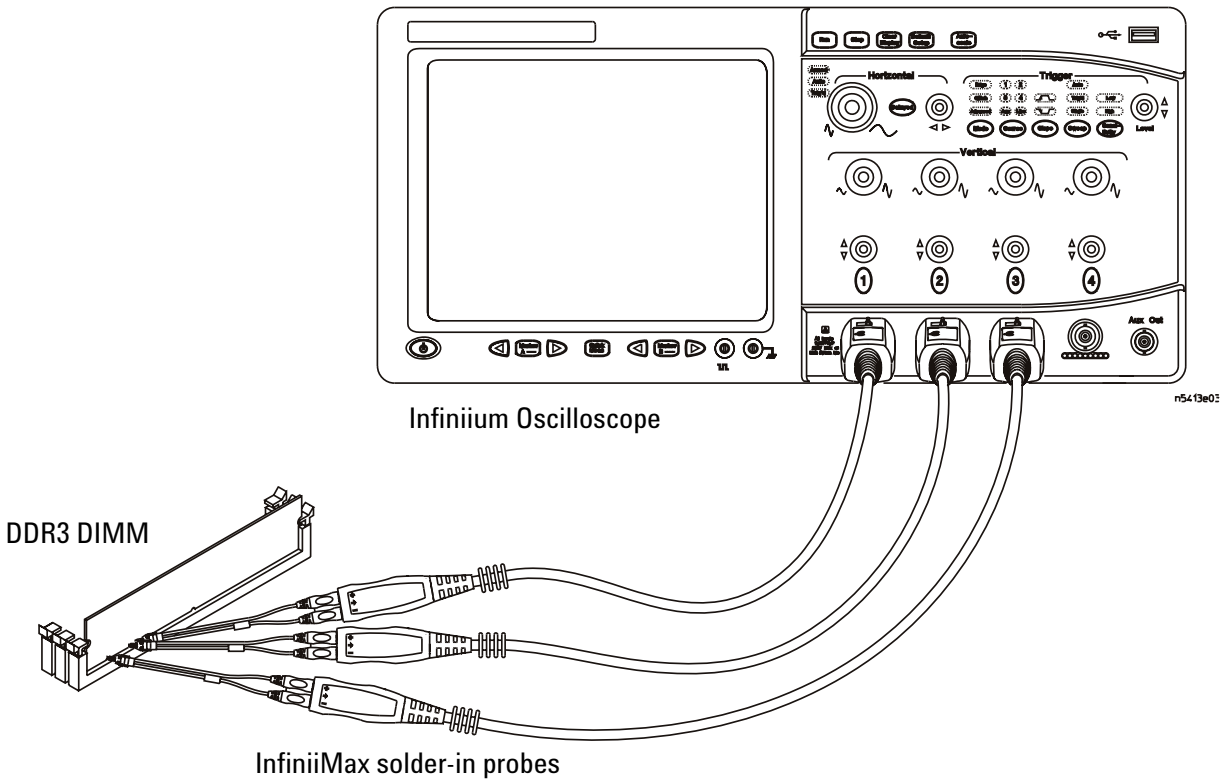


Figure 76 Probing for Command and Address Timing Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR3 Compliance Test Application. (The channels shown in Figure 76 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 16, “InfiniiMax Probing,” starting on page 261.

Test Procedure

1. Start the automated test application as described in “Starting the DDR3 Compliance Test Application" on page 27.
2. Ensure that the RAM reliability test software is running on the computer system where the DDR3 Device Under Test (DUT) is attached. This software will perform test on all the unused RAM on the system by producing repetitive burst of read-write data signals to the DDR3 memory.
3. Connect the differential solder-in probe head to the PUTs on the DDR3 DIMM.
4. Connect the oscilloscope probes to any channels of the oscilloscope.
5. In the DDR3 Test application, click the Set Up tab.
6. Select the Speed Grade options. For Command and Address Timing Tests, you can select any speed grade within the selection: DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600.
7. Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.
8. Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

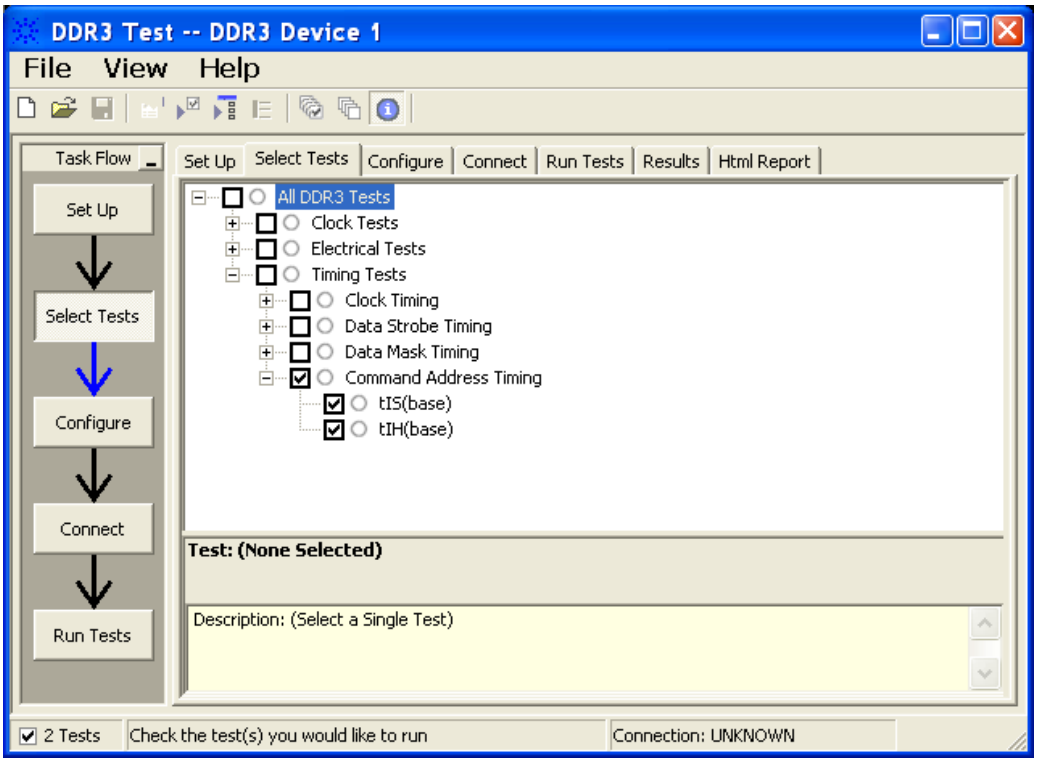


Figure 77 Selecting Command and Address Timing Tests

9 Follow the DDR3 Test application's task flow to set up the configuration options (see Table 55), run the tests and view the tests results.

Table 55 Test Configuration Options

Configuration Option	Description
Stop on error	Enabling this option will allow error messages to prompt whenever the test criteria is not met. Disabling this option will allow the system to bypass all the error messages that could occur and proceed to the next test. This option is suitable for long hours multiple trials.
Signal Threshold setting by percentage	This option allows you to define the Upper and Lower threshold of the signal by percentage.
VDD	Input supply voltage value.
VDDQ	Input supply voltage for data output.
Vref	Input reference voltage value.
Vih(DC)	Input voltage high value (direct current).
Vih(AC)	Input voltage high value (alternating current).
Vil(DC)	Input voltage low value (direct current).
Vil(AC)	Input voltage low value (alternating current).
Timing Tests	
Total Bit Display	Allows you to select the number of data bits to be displayed at the end of the test. Selecting more bits gives a better view of the entire burst of signals.
Total Measurement Required	To perform the total number of measurement based on your selection.
Channel (1,2,3)	Signal connected to the specific channel.
Option	Signal used for testing.
Signal selected	Signal connected to the specific channel.

tIS(base) - Address and Control Input Setup Time - Test Method of Implementation

The purpose of this test is to verify that the time interval from the address or control (rising or falling edge) setup time to the associated clock crossing edge is within the conformance limits as specified in the *JEDEC Standard JESD79-3*.

Figure 78 tIS(base) in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Read cycle only):

- Address and Control Signal (as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Address and Control Signal (as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Test Definition Notes from the Specification

Table 56 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
Command and Address setup time to CK, CK# referenced to Vih(ac)/Vil(ac) levels	tIS(base)	200	-	125	-	ps	b, 16

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
Command and Address setup time to CK, CK# referenced to Vih(ac)/Vil(ac) levels	tIS(base)	TBD	-	TBD	-	ps	b, 16

NOTE b, 16: Please refer to page 160, *JEDEC Standard JESD79-3*.

PASS Condition

The measured time interval between the address/control setup time and the respective clock crossing point should be within the specification limit.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the CK-DQS.
5. tIS measurement will compare the rising edge (address/control rising e.g. Vih_ac against associated clock crossing) OR falling edge (address/control falling e.g. Vil_ac against associated clock crossing).
6. Assign marker A for the clock signal while marker B for the data signal, for the final measurement result.
7. Measure delta of marker A and marker B and this will be the test result.
8. Compare the test result against the compliance test limit.

Test References

See Table 66 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79-3*.

tIH(base) - Address and Control Input Hold Time - Test Method of Implementation

The purpose of this test is to verify that the time interval from the address or control (rising or falling edge) hold time to the associated clock crossing edge is within the conformance limits as specified in the *JEDEC Standard JESD79-3*.

Figure 79 tIH(base) in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Read cycle only):

- Address and Control Signal (as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Address and Control Signal (as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Test Definition Notes from the Specification

Table 57 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
Command and Address hold time to CK, CK# referenced to Vih(ac)/Vil(ac) levels	tIH(base)	275	-	200	-	ps	b, 16

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
Command and Address hold time to CK, CK# referenced to Vih(ac)/Vil(ac) levels	tIH(base)	TBD	-	TBD	-	ps	b, 16

NOTE b, 16: Please refer to page 160, *JEDEC Standard JESD79-3*.

PASS Condition

The measured time interval between the address/control hold time and the respective clock crossing point should be within the specification limit.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the CK-DQS.
5. tIH measurement will compare the rising edge (address/control rising e.g. Vih_dc against associated clock crossing) OR falling edge (address/control falling e.g. Vil_dc against associated clock crossing).
6. Assign marker A for the clock signal while marker B for the data signal, for the final measurement result.
7. Measure delta of marker A and marker B and this will be the test result.
8. Compare the test result against the compliance test limit.

Test References

See Table 66 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79-3*.

13 Advanced Debug Mode Read-Write Eye-Diagram Tests

This section provides the Methods of Implementation (MOIs) for Advanced Debug Mode Read-Write Eye-Diagram tests using an Agilent 54850A series or 80000 series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR3 Compliance Test Application.

Probing for Advanced Debug Mode Read-Write Eye Diagram Tests

When performing the Advanced Debug Mode Read-Write Eye Diagram tests, the DDR3 Compliance Test Application will prompt you to make the proper connections as shown in Figure 80.

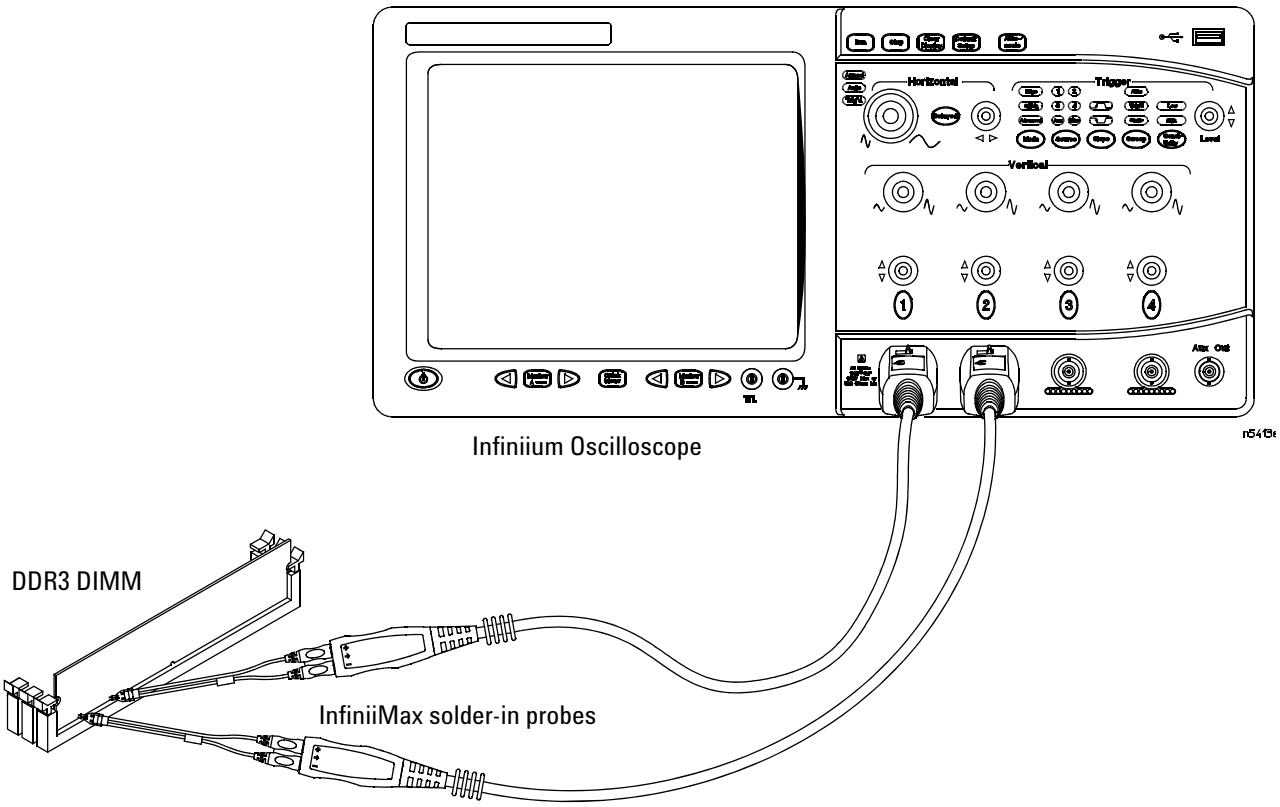


Figure 80 Probing for Advanced Debug Mode Read-Write Eye Diagram Tests

You can use any of the oscilloscope channels as the Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR3 Compliance Test Application. (The channels shown in Figure 80 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 16, “InfiniiMax Probing,” starting on page 261.

Test Procedure

1 Start the automated test application as described in "Starting the DDR3 Compliance Test Application" on page 27.

2 Ensure that the RAM reliability test software is running on the computer systems where the DDR3 Device Under Test (DUT) is attached. This software will perform a test on all the unused RAM on the system by producing repetitive bursts of read-write data signals to the DDR3 memory.

3 Connect the differential solder-in probe head to the PUTs on the DDR3 DIMM.

4 Connect the oscilloscope probes to any of the oscilloscope channels.

5 In the DDR3 Test application, click the Set Up tab.

6 Select Advanced Debug as the Test Mode option. This selection shows an additional command button - **Set Mask File**.

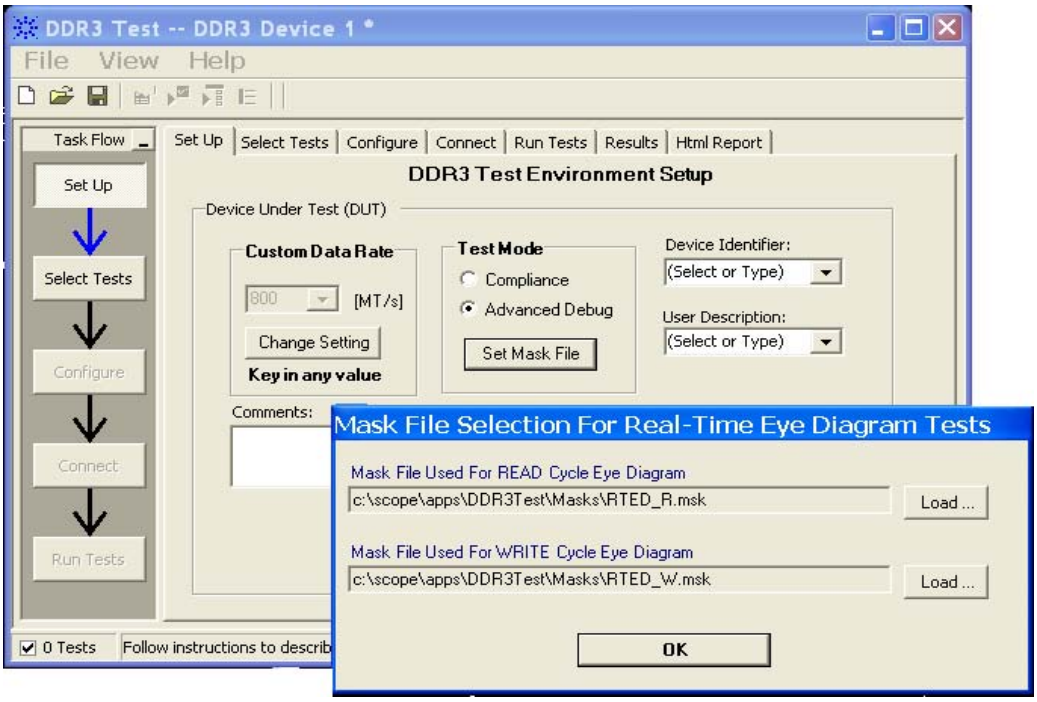


Figure 81 Selecting Advanced Debug Test Mode

7 Click this button to view or select test mask files for eye diagram tests.

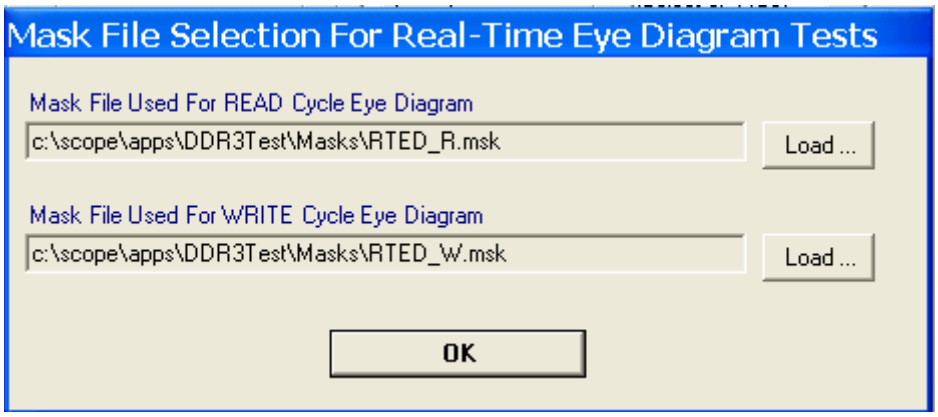


Figure 82 Selecting Test Mask for Eye Diagram Tests

8 Advanced Debug Mode also allows you to type in the data rate of the DUT signal.

9 Type in or select the Device Identifier as well as the User Description from the drop-down list. Enter your comments in the Comments text box.

10 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

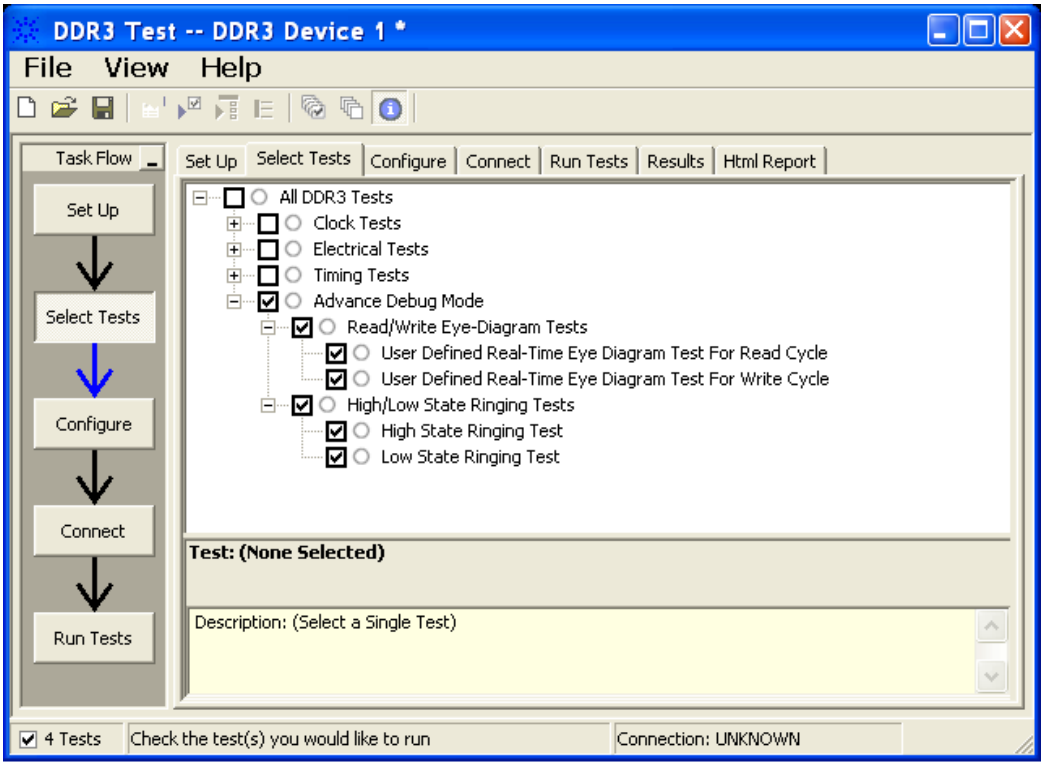


Figure 83 Selecting Advanced Debug Read-Write Eye-Diagram Tests

11 Follow the DDR3 Test application's task flow to set up the configuration options (see Table 58), run the tests and view the tests results.

Table 58 Test Configuration Options

Configuration Option	Description
Stop on error	Enabling this option will allow error messages to prompt whenever the test criteria is not met. Disabling this option will allow the system to bypass all the error messages that could occur and proceed to the next test. This option is suitable for long hours multiple trials.
Signal Threshold setting by percentage	This option allows you to define the Upper and Lower threshold of the signal by percentage.
VDD	Input supply voltage value.
VDDQ	Input supply voltage for data output.
Vref	Input reference voltage value.
Vih(DC)	Input voltage high value (direct current).
Vih(AC)	Input voltage high value (alternating current).
Vil(DC)	Input voltage low value (direct current).
Vil(AC)	Input voltage low value (alternating current).
Read/Write Eye Diagram Tests	
Data Lane	Identifies the data lane for the eye diagram tests.
Data Source	Identifies the source of the data to be analyzed for eye diagram tests.
Data Strobe Lane	Identifies the data strobe lane for the eye diagram tests.
Data Strobe Source	Identifies the source of the data strobe for eye diagram tests.
Total Waveform	Select or type the total number of waveforms required for eye diagram tests.
Re-scale Test Mask	You may enable or disable horizontal re-scaling option of the selected test mask to be loaded in the eye diagram tests.
InfiniiScan Limits	
Read Cycle	
IScan_UL_READ	Identifies the upper limit for Setup Time measurement used in the InfiniiScan Measurement Mode (READ cycle)
IScan_LL_READ	Identifies the lower limit for Setup Time measurement used in the InfiniiScan Measurement Mode (READ cycle)
Write Cycle	
IScan_UL_WRITE	Identifies the upper limit for Setup Time measurement used in the InfiniiScan Measurement Mode (WRITE cycle)
IScan_LL_WRITE	Identifies the lower limit for Setup Time measurement used in the InfiniiScan Measurement Mode (WRITE cycle)

User Defined Real-Time Eye Diagram Test for Read Cycle Method of Implementation

The Advanced Debug Mode Read-Write Eye Diagram test can be divided into two sub-tests. One of them is the User Defined Real-Time Eye Diagram Test for Read Cycle. There is no available specification on the eye test in *JEDEC Standard JESD79-3* specifications. Mask testing is definable by the customers for their evaluation tests purpose. The purpose of this test is to automate all the required setup procedures in order to generate an eye diagram for the DDR3 data READ cycle. This additional feature of mask test allows you to perform evaluation and debugging on the created eye diagram. The test will show a fail status if the total failed waveforms is greater than 0.

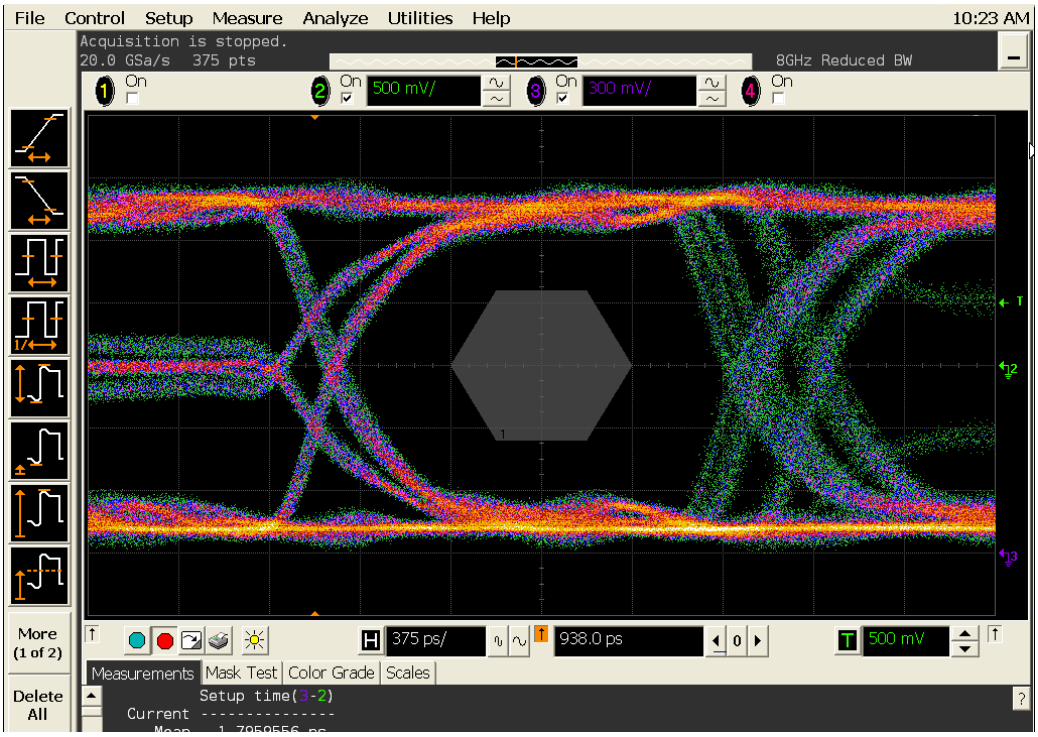


Figure 84 Eye Diagram Tests for Read Cycle

Signals of Interest

Based on the test definition (Read cycle only):

- Data Signal

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)

- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

Measurement Algorithm

1. Set the termination condition of the mask test to "Waveforms" with the number of waveforms to be acquired.
2. Start mask test.
3. Loop until number of required waveforms are acquired.
4. Obtain and display total failed waveforms as the test result.

User Defined Real-Time Eye Diagram Test for Write Cycle Method of Implementation

Just as in the previous test, there is no available specification on the eye diagram test in the *JEDEC Standard JESD79-3* specifications for User Defined Real-Time Eye Diagram Test for Write Cycle. Mask testing is definable by the customers for their evaluation tests purpose. The purpose of this test is to automate all the required setup procedures in order to generate an eye diagram for the DDR3 data WRITE cycle. This additional feature of mask test allows you to perform evaluation and debugging on the created eye diagram. The test will show a fail status if the total failed waveforms is greater than 0.

.

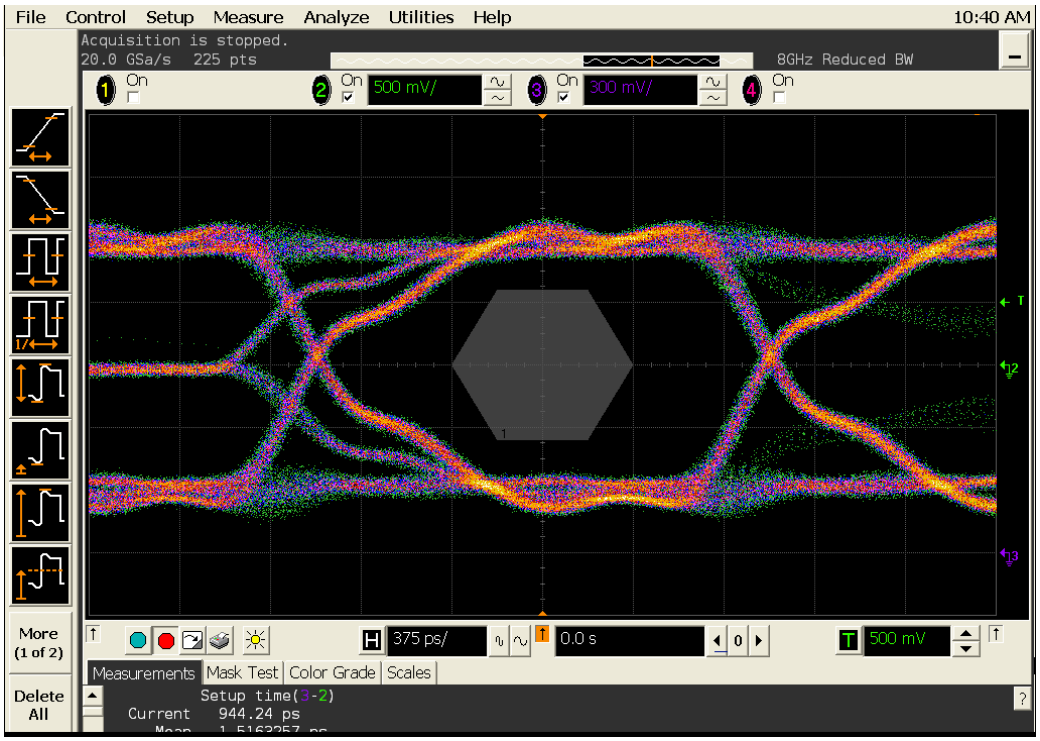


Figure 85 Eye Diagram Tests for Write Cycle

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)

- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

Measurement Algorithm

1. Set the termination condition of the mask test to "Waveforms" with the number of waveforms to be acquired.
2. Start mask test.
3. Loop until number of required waveforms are acquired.
4. Obtain and display total failed waveforms as the test result.

14 Advance Debug Mode High-Low State Ringing Tests

This section provides the Methods of Implementation (MOIs) for Advanced Debug Mode High-Low State Ringing tests using an Agilent 54850A series or 80000 series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR3 Compliance Test Application.

Probing for Advanced Debug Mode High-Low State Ringing Tests

When performing the intra-pair skew tests, the DDR3 Compliance Test Application will prompt you to make the proper connections as shown in Figure 86.

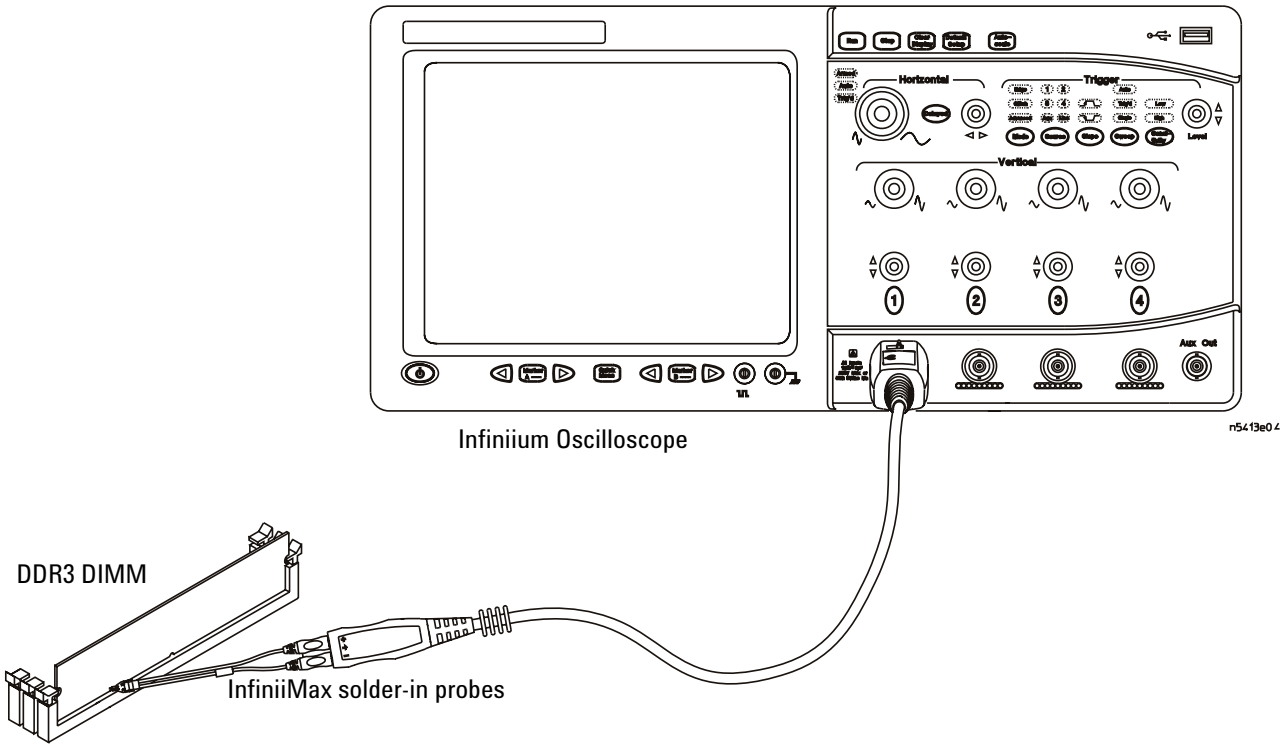


Figure 86 Probing for Advanced Debug Mode High-Low State Ringing Tests

You can use any of the oscilloscope channels as the Pin Under Test (PUT) source channel. You identify the channels used for each signal in the Configuration tab of the DDR3 Compliance Test Application. (The channel shown in Figure 86 is just an example).

For more information on the probe amplifiers and differential probe heads, see Chapter 16, “InfiniiMax Probing,” starting on page 261.

Test Procedure

1 Start the automated test application as described in "Starting the DDR3 Compliance Test Application" on page 27.

2 Ensure that the RAM reliability test software is running on the computer systems where the DDR3 Device Under Test (DUT) is attached. This software will perform tests on all the unused RAM in the system by producing repetitive bursts of read-write data signals to the DDR3 memory.

3 Connect the differential solder-in probe head to the PUT on the DDR3 DIMM.

4 Connect the oscilloscope probes to any of the oscilloscope channels.

5 In the DDR3 test application, click the Set Up tab.

6 Select Advanced Debug as the Test Mode option. This selection shows an additional command button - **Set Mask File**. This is only relevant for Read-Write Eye-Diagram.

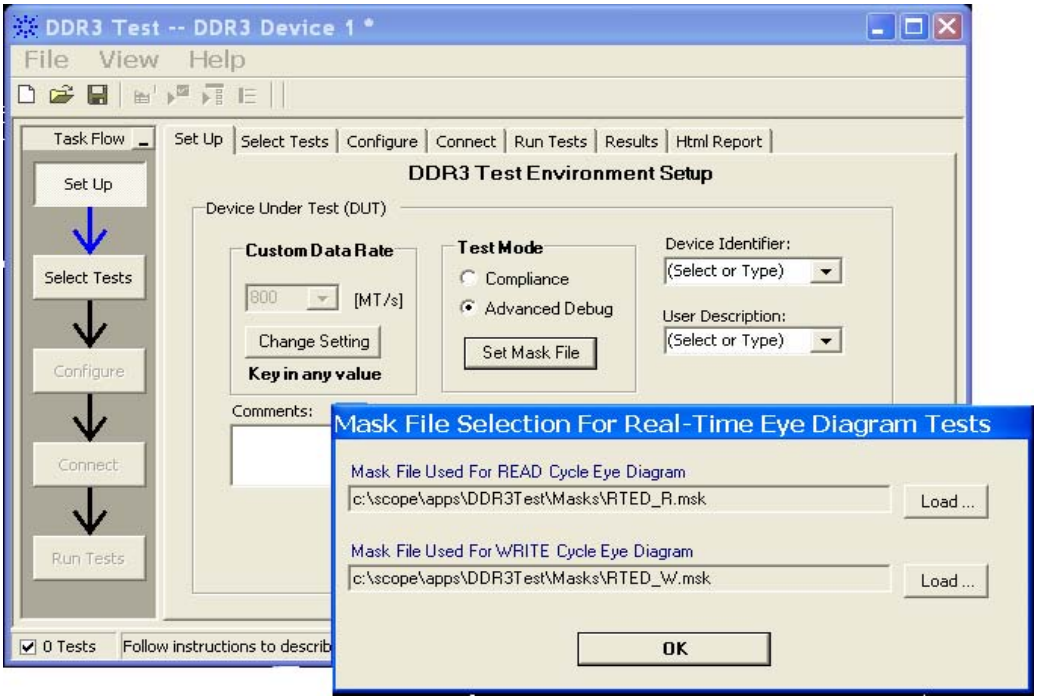


Figure 87 Selecting Advanced Debug Test Mode

7 Advanced Debug Mode also allows you to type in the data rate of the DUT signal.

8 Type in or select the Device Identifier as well as the User Description from the drop-down list. Enter your comments in the Comments text box.

9 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

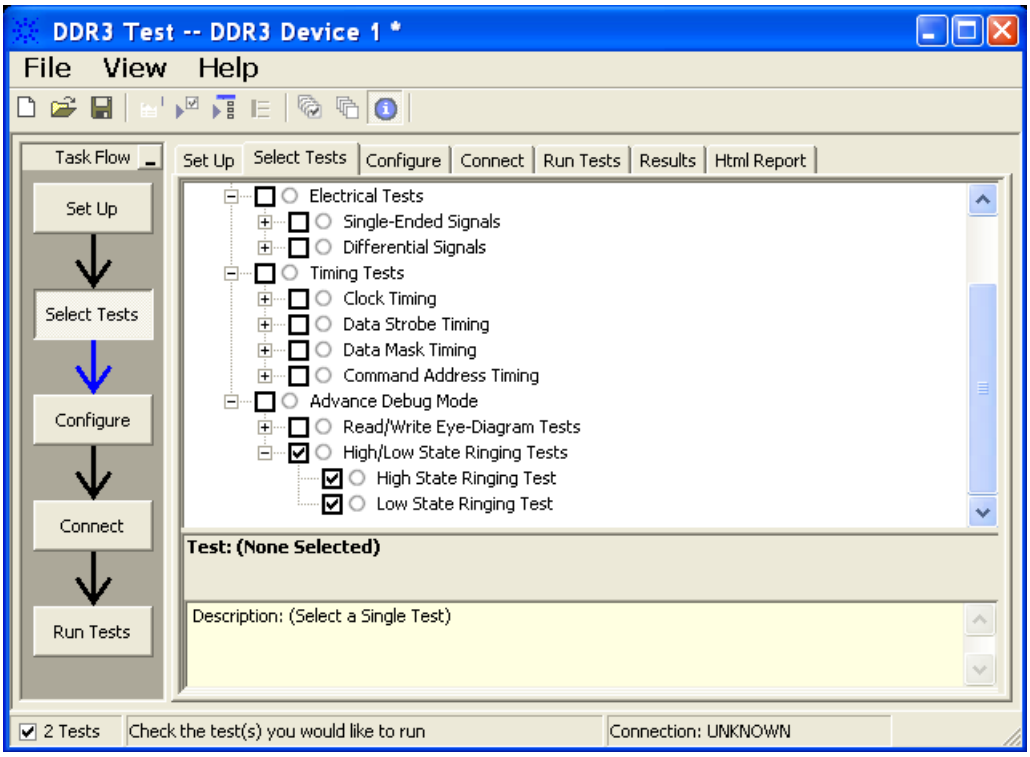


Figure 88 Selecting Advanced Debug High-Low State Ringing Tests

10 Follow the DDR3 Test application's task flow to set up the configuration options (see Table 59), run the tests and view the tests results.

Table 59 Test Configuration Options

Configuration Option	Description
Stop on error	Enabling this option will allow error messages to prompt whenever the test criteria is not met. Disabling this option will allow the system to bypass all the error messages that could occur and proceed to the next test. This option is suitable for long hours multiple trials.
Signal Threshold setting by percentage	This option allows you to define the Upper and Lower threshold of the signal by percentage.
VDD	Input supply voltage value.
VDDQ	Input supply voltage for data output.
Vref	Input reference voltage value.
Vih(DC)	Input voltage high value (direct current).
Vih(AC)	Input voltage high value (alternating current).
Vil(DC)	Input voltage low value (direct current).
Vil(AC)	Input voltage low value (alternating current).
High/Low State Ringing Tests	
Pin Under Test, PUT	Identifies the Pin Under Test for High-Low State Ringing tests.
PUT Source	Identifies the source of the PUT for High-Low State Ringing Tests.
Time-out	Identifies the time-out value to be used for High-Low State Ringing Test.
Trigger Level	Sets the rising edge voltage level to trigger on for all High-Low State Ringing Test.
High/Low State	
Upper Level	Identifies the upper threshold level to be used for the ringing tests.
Hysteresis	Identifies the hysteresis value to be used for the ringing test.
Lower Level	Identifies the lower threshold level to be used for the ringing tests.

High State Ringing Tests Method of Implementation

The Advanced Debug Mode Ringing test can be divided into two sub-tests. One of them is the High State Ringing test. There is no available specification for this test in the *JEDEC Standard JESD79-3* specifications. The ringing debug test is definable by the customers to capture the glitch of interest for the logic high state section in a test signal for evaluation purposes. The purpose of this test is to automate all the required setup procedures, particularly the InfiniiScan RUNT mode setup, to capture the ringing section of a test signal. Users are required to customize the threshold value in the Configure tab to capture the specific RUNT signals. The expected results are signals captured on the screen that fulfill the InfiniiScan RUNT criteria. There is a pulse in the captured signal that passes through two voltage level threshold but not the third.

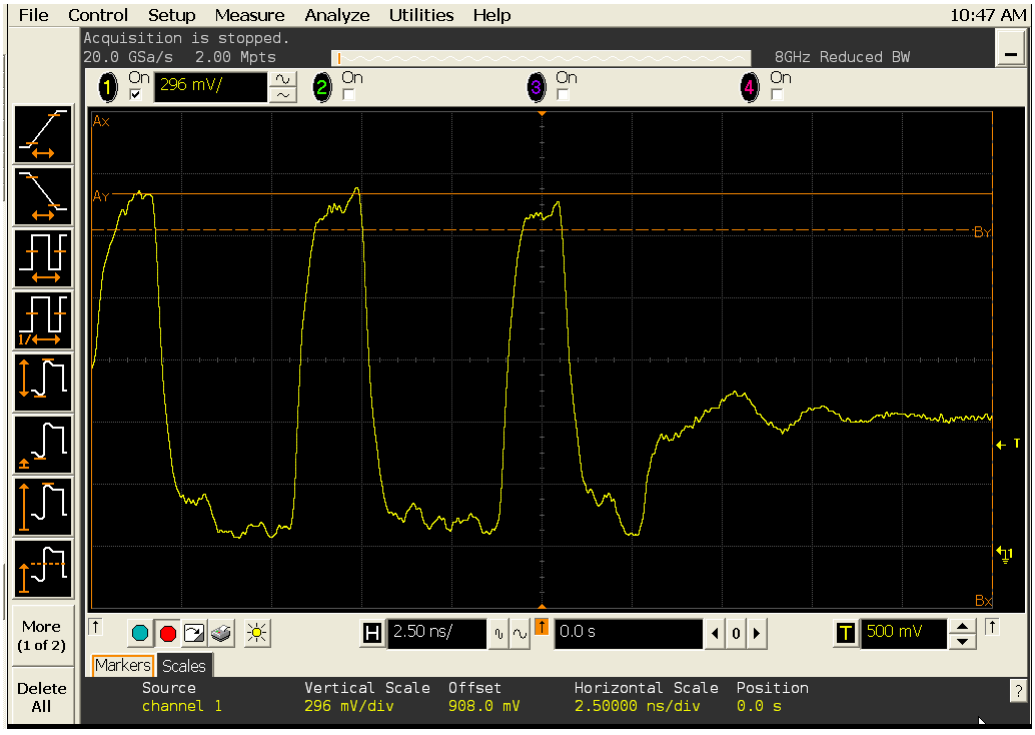


Figure 89 High State Ringing Test

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signals OR
- Data Strobe Signals OR
- Address Signals OR
- Control Signal OR
- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)*
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against the user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

Measurement Algorithm

1. Acquire initial signal data and then perform signal conditioning to maximize the screen resolution - vertical scale adjustment.
2. Setup the InfiniiScan to activate the RUNT mode.
3. Acquire test data with the InfiniiScan RUNT activated.
4. Display Markers to show the RUNT Upper Level and RUNT Lower Level.

Low State Ringing Tests Method of Implementation

Just as the High State Ringing test, there is no available specification in the *JEDEC Standard JESD79-3* specifications for the Low State Ringing tests. The ringing debug test is definable by the customers to capture the glitch of interest for the logic low state section in a test signal for evaluation purposes. The purpose of this test is to automate all the required setup procedures, particularly the InfiniiScan RUNT mode setup, to capture the ringing section of a test signal. Users are required to customize the threshold value in the Configure tab to capture the specific RUNT signals. The expected results are signals captured on the screen that fulfill the InfiniiScan RUNT criteria. There is a pulse in the captured signal that passes through two voltage level threshold but not the third.

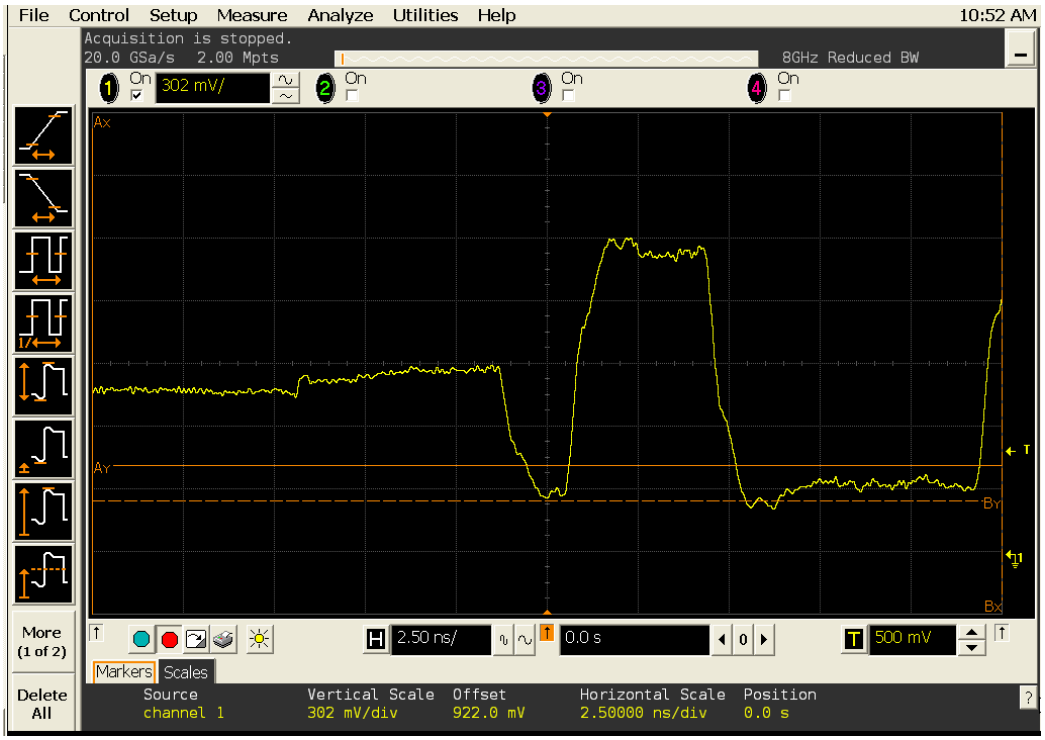


Figure 90 Low State Ringing Test

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signals OR
- Data Strobe Signals OR
- Address Signals OR
- Control Signal OR
- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)*
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

Measurement Algorithm

1. Acquire initial signal data and then perform signal conditioning to maximize the screen resolution - vertical scale adjustment.
2. Setup the InfiniiScan to activate the RUNT mode.
3. Acquire test data with the InfiniiScan RUNT activated.
4. Display Markers to show the RUNT Upper Level and RUNT Lower Level.

15 Calibrating the Infiniium Oscilloscope and Probe

This section describes the Agilent Infiniium digital storage oscilloscope calibration procedures.

Required Equipment for Oscilloscope Calibration

To calibrate the Infiniium oscilloscope in preparation for running the DDR3 automated tests, you need the following equipment:

- Keyboard, qty = 1, (provided with the Agilent Infiniium oscilloscope).
- Mouse, qty = 1, (provided with the Agilent Infiniium oscilloscope).
- Precision 3.5 mm BNC to SMA male adapter, Agilent p/n 54855-67604, qty = 2 (provided with the Agilent Infiniium oscilloscope).
- Calibration cable (provided with the 54850A series and 80000 series Infiniium oscilloscopes). Use a good quality 50 Ω BNC cable.
- BNC shorting cap (provided with the 54850A series Infiniium oscilloscopes).

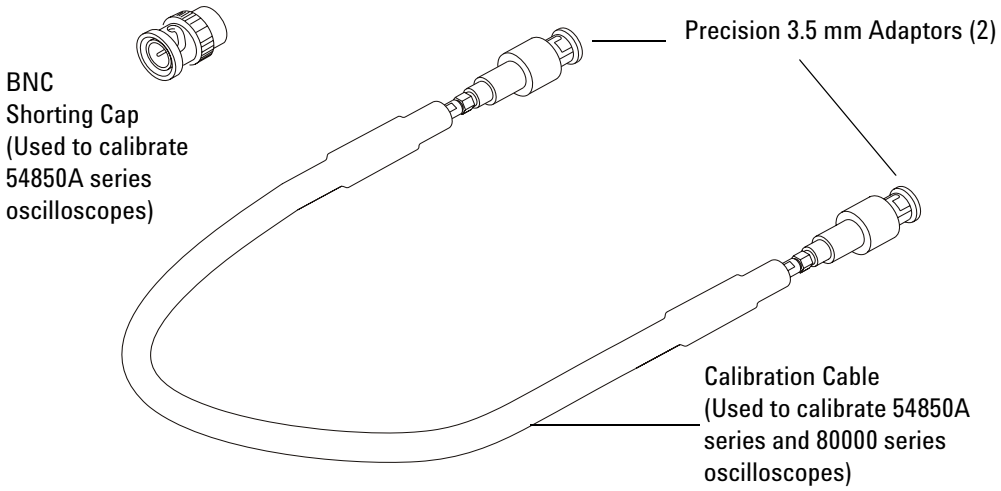


Figure 91 Accessories Provided with the Agilent Infiniium Oscilloscope

Internal Calibration

This will perform an internal diagnostic and calibration cycle for the oscilloscope. For the Agilent oscilloscope, this is referred to as Calibration. This Calibration will take about 20 minutes. Perform the following steps:

1 Set up the oscilloscope with the following steps:

   a Connect the keyboard, mouse, and power cord to the rear of the oscilloscope.

   b Plug in the power cord.

   c Turn on the oscilloscope by pressing the power button located on the lower left of the front panel.

   d Allow the oscilloscope to warm up at least 30 minutes prior to starting the calibration procedure in step 3 below.

2 Locate and prepare the accessories that will be required for the internal calibration:

   a Locate the BNC shorting cap.

   b Locate the calibration cable.

   c Locate the two Agilent precision SMA/BNC adapters.

   d Attach one SMA adapter to the other end of the calibration cable - hand tighten snugly.

   e Attach another SMA adapter to the other end of the calibration cable - hand tighten snugly.

3 Referring to Figure 92 below, perform the following steps:

   a Click on the Utilities>Calibration menu to open the Calibration dialog box.

Figure 92 Accessing the Calibration Menu

4 Referring to Figure 93 below, perform the following steps to start the calibration:

   b Uncheck the Cal Memory Protect checkbox.

   c Click the Start button to begin the calibration.

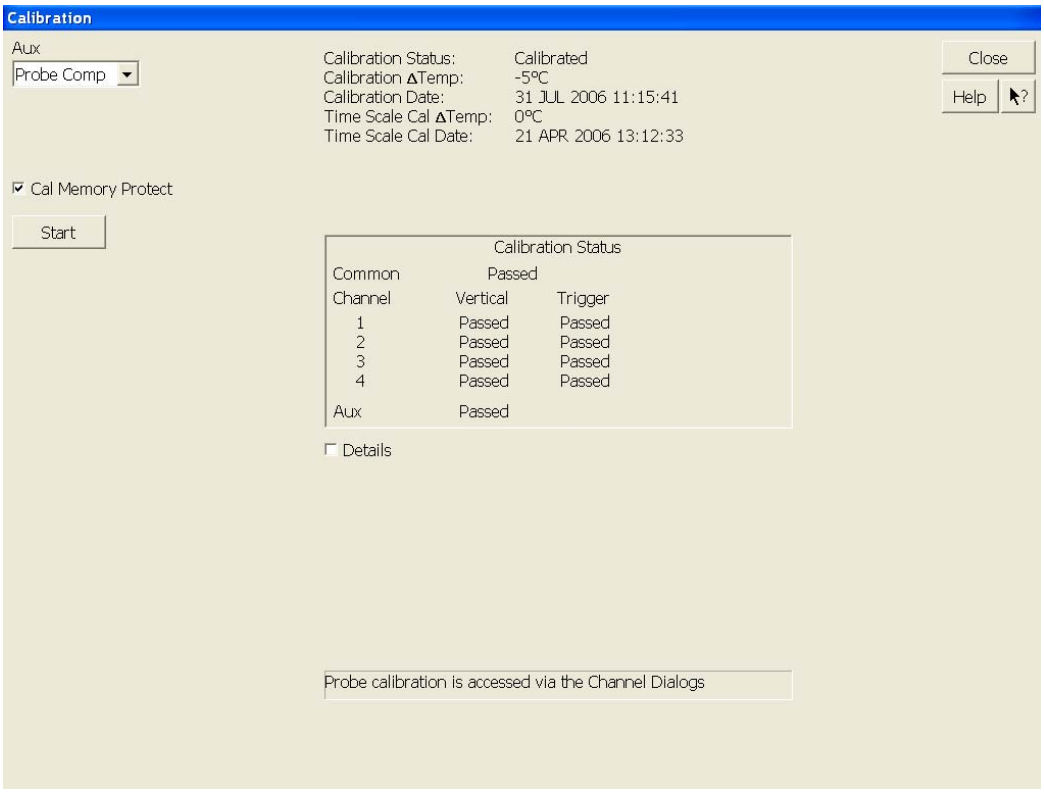


Figure 93 Oscilloscope Calibration Window

d During the calibration of channel 1, if you are prompted to perform a Time Scale Calibration, as shown in Figure 94 below.

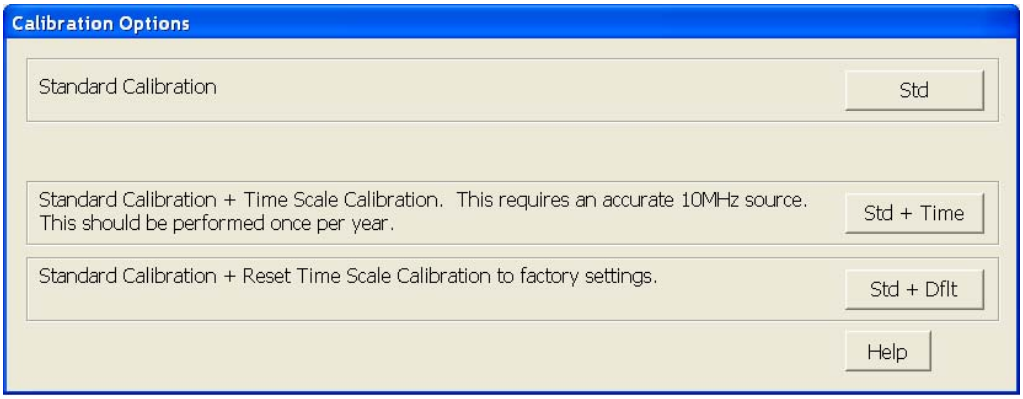


Figure 94 Time Scale Calibration Dialog box

e Click on the Std+Dflt button to continue the calibration, using the Factory default calibration factors.

f When the calibration procedure is complete, you will be prompted with a Calibration Complete message window. Click the OK button to close this window.

g Confirm that the Vertical and Trigger Calibration Status for all Channels passed.

h Click the Close button to close the calibration window.

i The internal calibration is completed.

j Read NOTE below.

NOTE These steps do not need to be performed every time a test is run. However, if the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, this calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the Utilities>Calibration menu.

Required Equipment for Probe Calibration

Before performing DDR3 tests you should calibrate the probes. Calibration of the solder-in probe heads consist of a vertical calibration and a skew calibration. The vertical calibration should be performed before the skew calibration. Both calibrations should be performed for best probe measurement performance.

The calibration procedure requires the following parts.

- BNC (male) to SMA (male) adaptor
- Deskew fixture
- 50 Ω SMA terminator

Probe Calibration

Connecting the Probe for Calibration

For the following procedure, refer to Figure 95 below.

1. Connect BNC (male) to SMA (male) adaptor to the deskew fixture on the connector closest to the yellow pincher.
2. Connect the 50 Ω SMA terminator to the connector farthest from yellow pincher.
3. Connect the BNC side of the deskew fixture to the Aux Out BNC of the Infiniium oscilloscope.
4. Connect the probe to an oscilloscope channel.
5. To minimize the wear and tear on the probe head, it should be placed on a support to relieve the strain on the probe head cables.
6. Push down the back side of the yellow pincher. Insert the probe head resistor lead underneath the center of the yellow pincher and over the center conductor of the deskew fixture. The negative probe head resistor lead or ground lead must be underneath the yellow pincher and over one of the outside copper conductors (ground) of the deskew fixture. Make sure that the probe head is approximately perpendicular to the deskew fixture.
7. Release the yellow pincher.

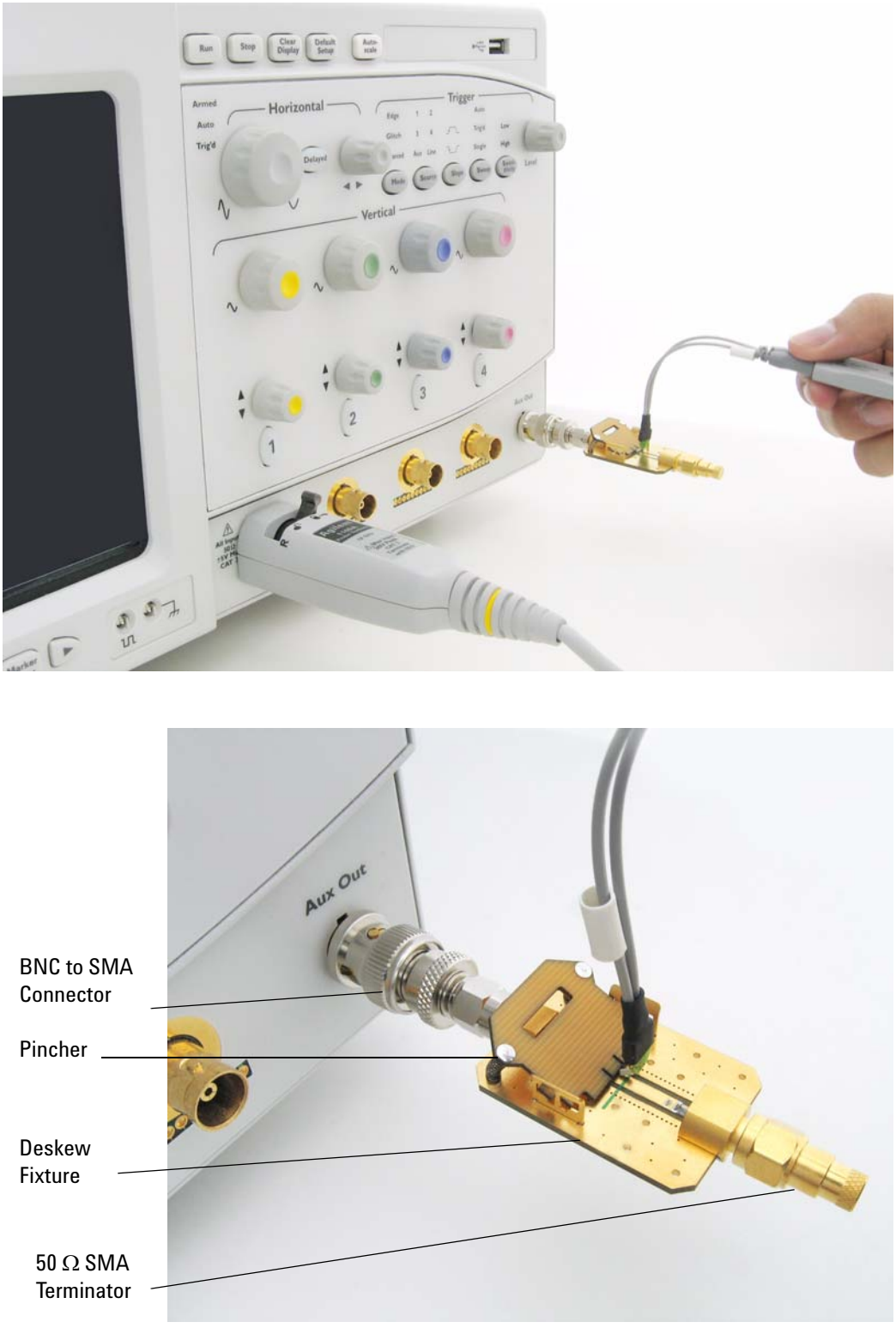


Figure 95 Solder-in Probe Head Calibration Connection Example

Verifying the Connection

1 On the Infiniium oscilloscope, press the autoscale button on the front panel.

2 Set the volts per division to 100 mV/div.

3 Set the horizontal scale to 1.00 ns/div.

4 Set the horizontal position to approximately 3 ns. You should see a waveform similar to that in Figure 96 below.

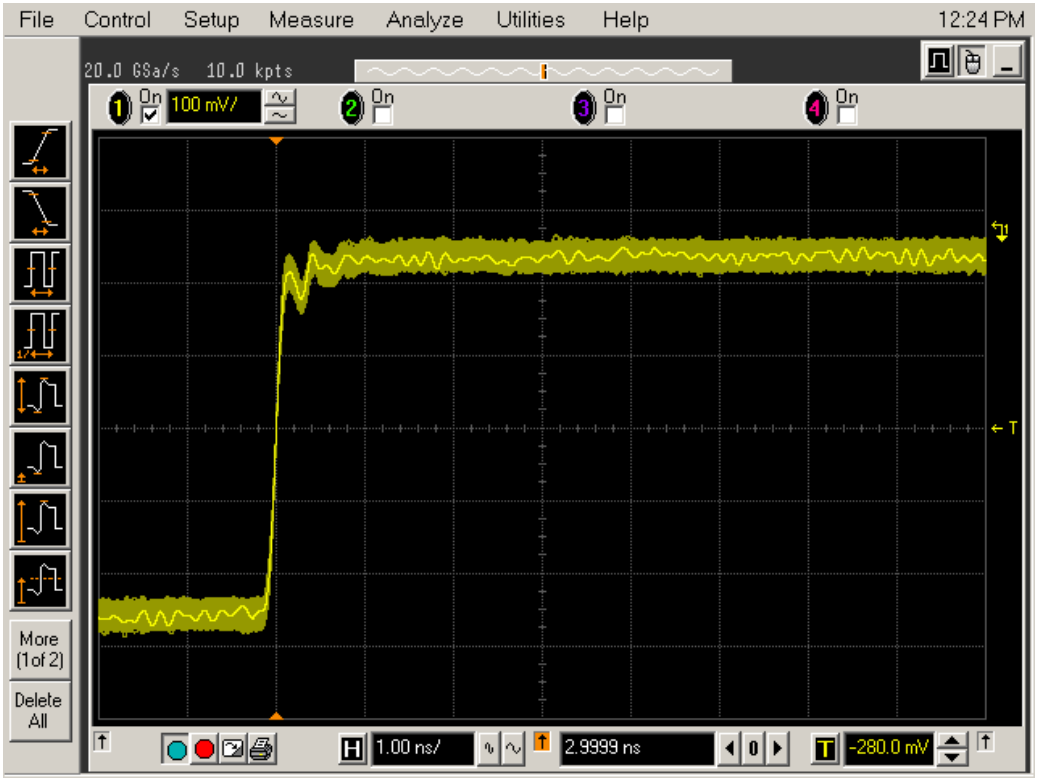


Figure 96 Good Connection Waveform Example

If you see a waveform similar to that of Figure 97 below, then you have a bad connection and should check all of your probe connections.

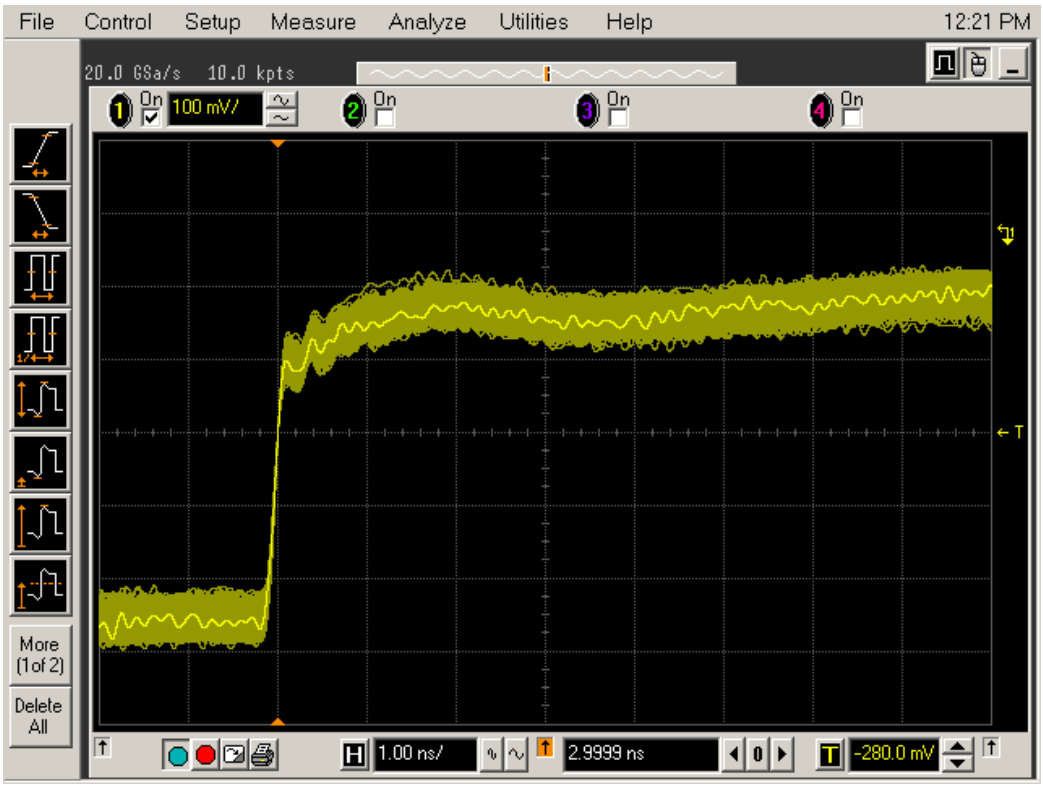


Figure 97 Bad Connection Waveform Example

Running the Probe Calibration and Deskew

1 On the Infiniium oscilloscope in the Setup menu, select the channel connected to the probe, as shown in Figure 98.

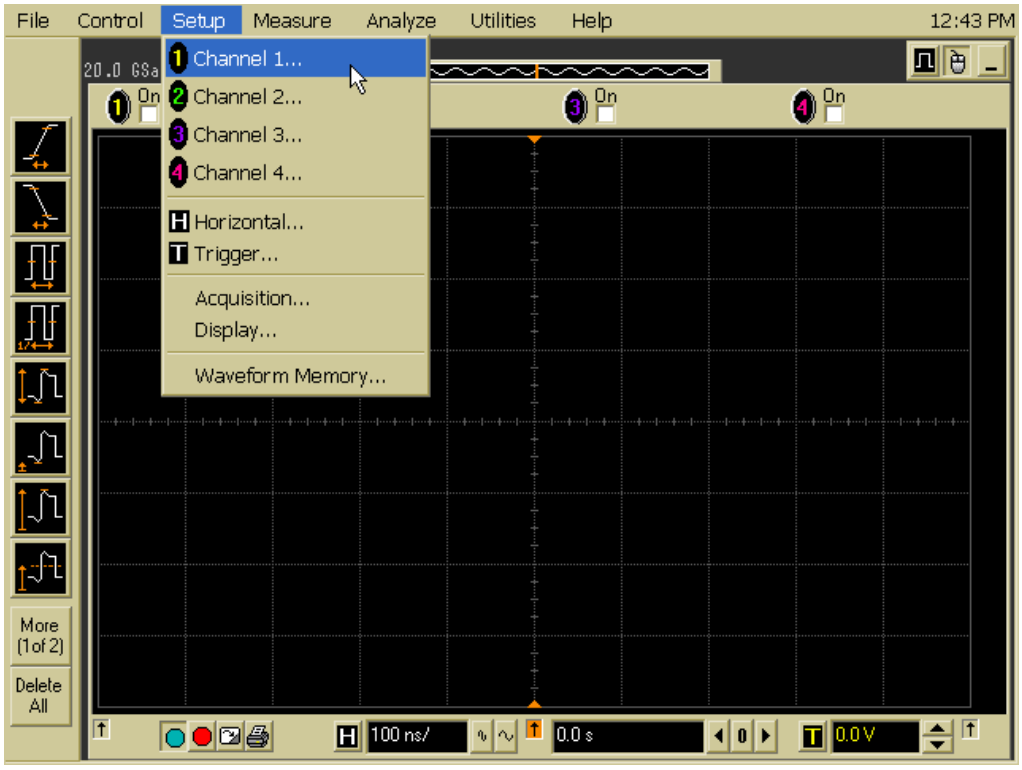


Figure 98 Channel Setup Window.

2 In the Channel Setup dialog box, select the Probes... button, as shown in Figure 99.

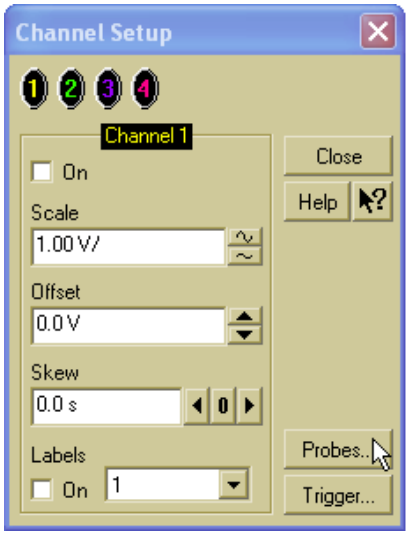


Figure 99 Channel Dialog Box

3 In the Probe Setup dialog box, select the Calibrate Probe... button.

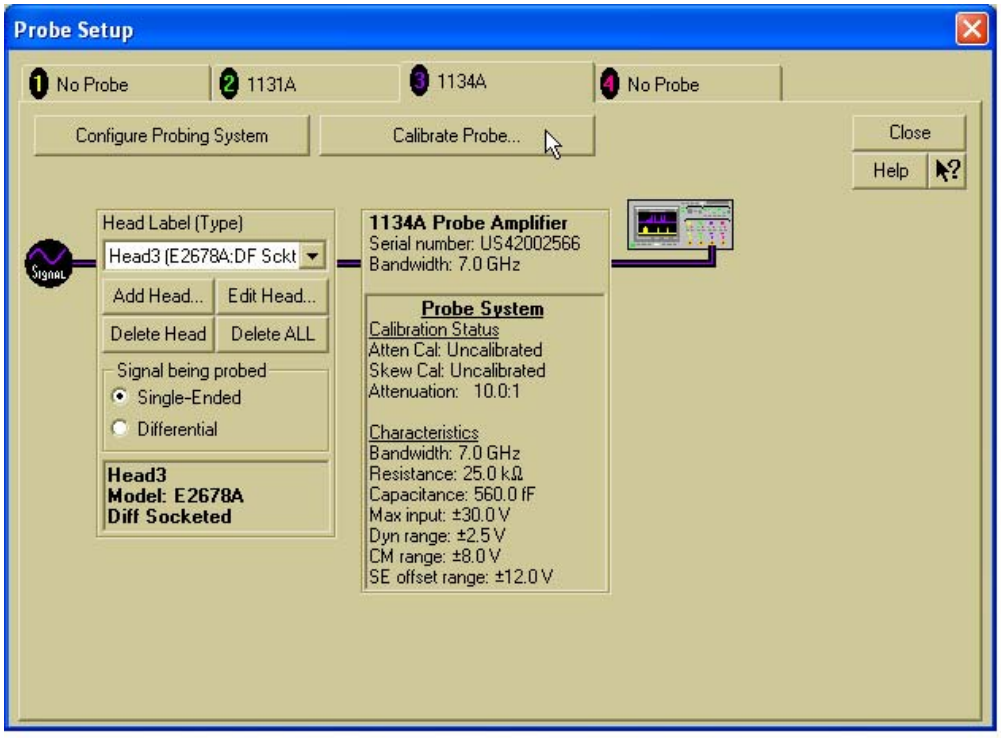


Figure 100 Probe Setup Window.

4 In the Probe Calibration dialog box, select the Calibrated Atten/Offset radio button.

5 Select the Start Atten/Offset Calibration... button and follow the on-screen instructions for the vertical calibration procedure.

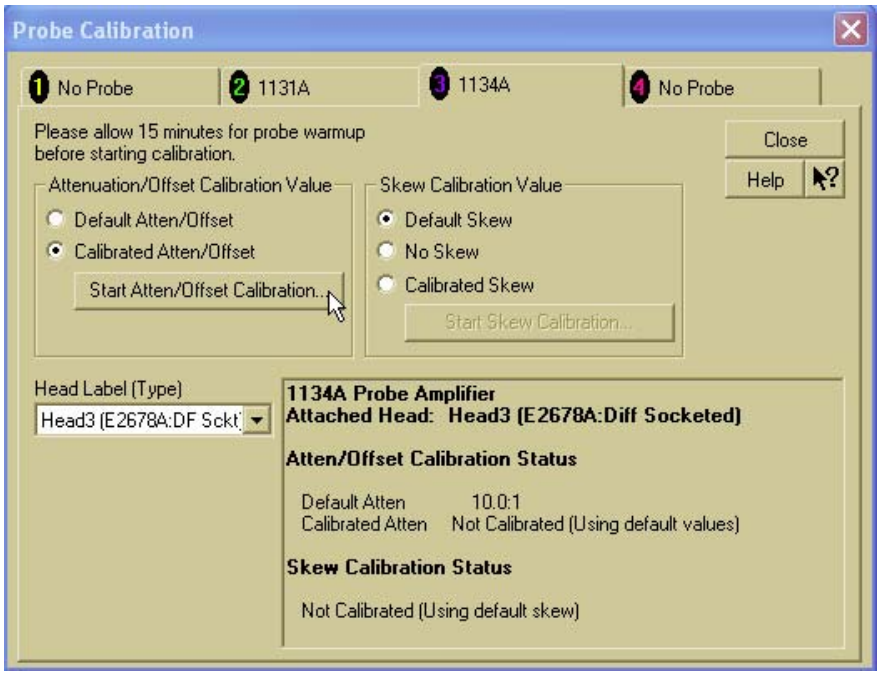


Figure 101 Probe Calibration Window.

6 Once the vertical calibration has successfully completed, select the Calibrated Skew... button.

7 Select the Start Skew Calibration... button and follow the on-screen instructions for the skew calibration.

At the end of each calibration, the oscilloscope will prompt you if the calibration was or was not successful.

Verifying the Probe Calibration

If you have successfully calibrated the probe, it is not necessary to perform this verification. However, if you want to verify that the probe was properly calibrated, the following procedure will help you verify the calibration.

The calibration procedure requires the following parts:

- BNC (male) to SMA (male) adaptor
- SMA (male) to BNC (female) adaptor
- BNC (male) to BNC (male) 12 inch cable such as the Agilent 8120-1838

- Agilent 54855-61620 calibration cable (Infiniium oscilloscopes with bandwidths of 6 Ghz and greater only)
- Agilent 54855-67604 precision 3.5 mm adaptors (Infiniium oscilloscopes with bandwidths of 6 Ghz and greater only)
- Deskew fixture

For the following procedure, refer to Figure 102.

1 Connect BNC (male) to SMA (male) adaptor to the deskew fixture on the connector closest to the yellow pincher.

2 Connect the SMA (male) to BNC (female) to the connector farthest from the yellow pincher.

3 Connect the BNC (male) to BNC (male) cable to the BNC connector on the deskew fixture to one of the unused oscilloscope channels. For infiniium oscilloscopes with bandwidths of 6 GHz and greater, use the 54855-61620 calibration cable and the two 54855-64604 precision 3.5 mm adaptors.

4 Connect the BNC side of the deskew fixture to the Aux Out BNC of the Infiniium oscilloscope.

5 Connect the probe to an oscilloscope channel.

6 To minimize the wear and tear on the probe head, it should be placed on a support to relieve the strain on the probe head cables.

7 Push down on the back side of the yellow pincher. Insert the probe head resistor lead underneath the center of the yellow pincher and over the center conductor of the deskew fixture. The negative probe head resistor lead or ground lead must be underneath the yellow pincher and over one of the outside copper conductors (ground) of the deskew fixture. Make sure that the probe head is approximately perpendicular to the deskew fixture.

8 Release the yellow pincher.

9 On the oscilloscope, press the autoscale button on the front panel.

10 Select Setup menu and choose the channel connected to the BNC cable from the pull-down menu.

11 Select the Probes... button.

12 Select the Configure Probe System button.

13 Select User Defined Probe from the pull-down menu.

14 Select the Calibrate Probe... button.

15 Select the Calibrated Skew radio button.

16 Once the skew calibration is completed, close all dialog boxes.

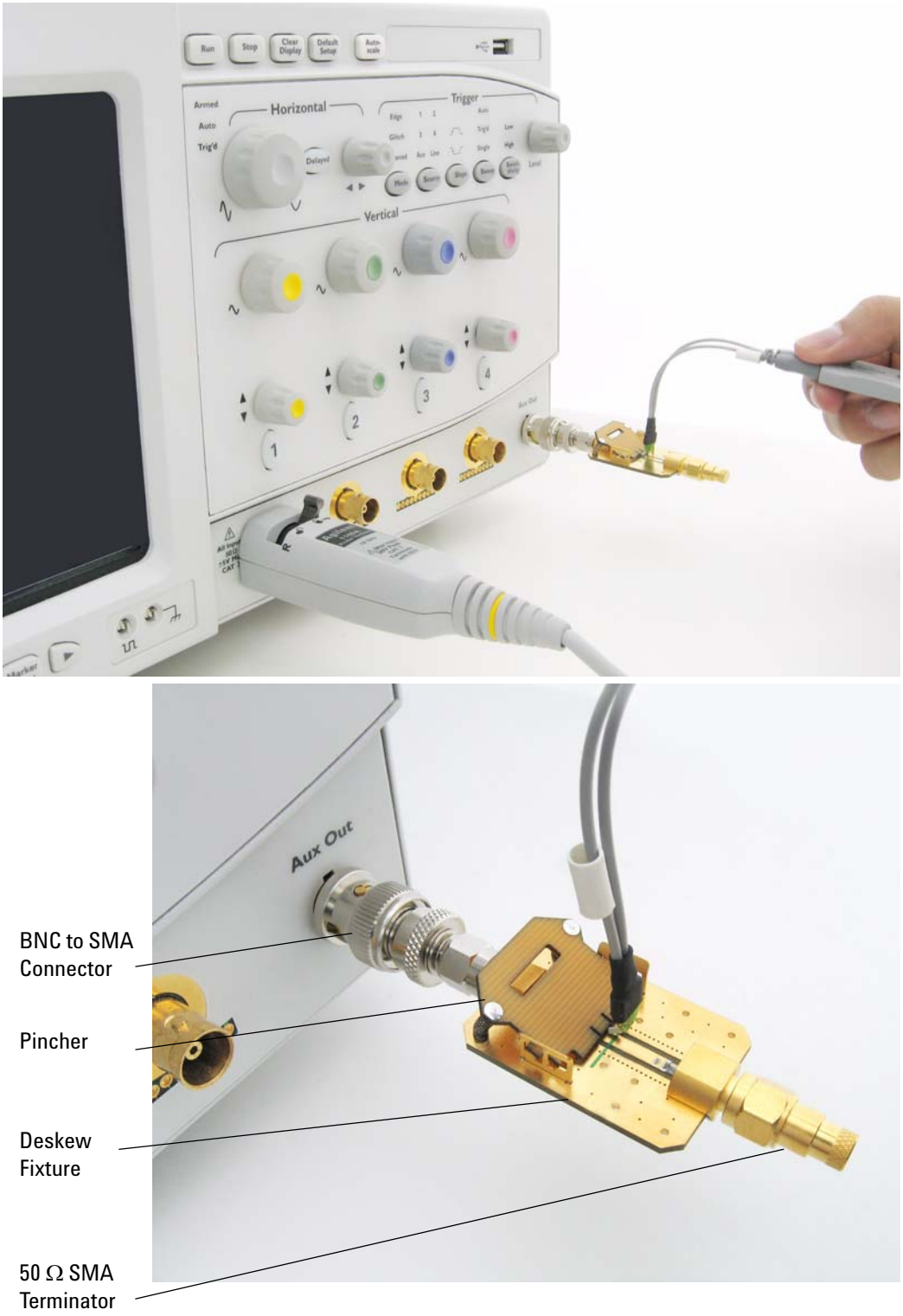


Figure 102 Probe Calibration Verification Connection Example

17 Select the Start Skew Calibration... button and follow the on-screen instructions.

18 Set the vertical scale for the displayed channels to 100 mV/div.

19 Set the horizontal range to 1.00 ns/div.

20 Set the horizontal position to approximately 3 ns.

21 Change the vertical position knobs of both channels until the waveforms overlap each other.

22 Select the Setup menu choose Acquisition... from the pull-down menu.

23 In the Acquisition Setup dialog box enable averaging. When you close the dialog box, you should see waveforms similar to that in Figure 103.

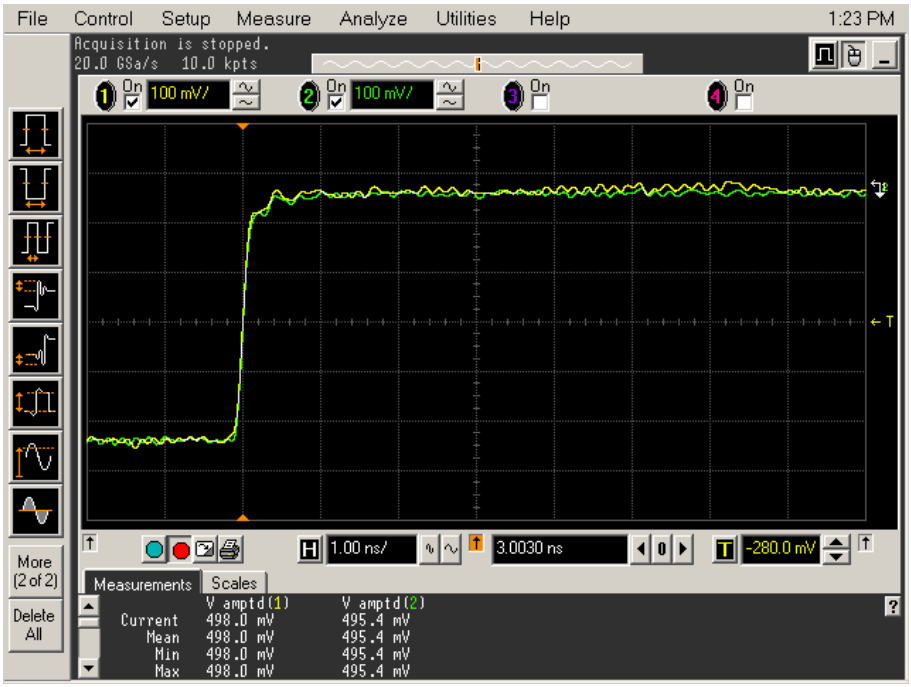


Figure 103 Calibration Probe Waveform Example

NOTE

Each probe is calibrated with the oscilloscope channel to which it is connected. Do not switch probes between channels or other oscilloscopes, or it will be necessary to calibrate them again. It is recommended that the probes be labeled with the channel on which they were calibrated.

16 InfiniiMax Probing

Figure 104 1134A InfiniiMax Probe Amplifier

Agilent recommends 116xA or 113xA probe amplifiers, which range from 3.5 GHz to 12 GHz.

Agilent also recommends the E2677A differential solder-in probe head. Other probe head options include N5381A InfiniiMax II 12 GHz differential solder-in probe head, N5382A InfiniiMax II 12 GHz differential browser, E2675A InfiniiMax differential browser probe head, N5425A InfiniiMax ZIF probe head and N5426A ZIF Tips.

Figure 105 E2677A / N5381A Differential Solder-in Probe Head

Table 60 Probe Head Characteristics (with 1134A probe amplifier)

Probe Head	Model Number	Differential Measurement (BW, input C, input R)	Single-Ended Measurement (BW, input C, input R)
Differential Solder-in	E2677A	7 GHz, 0.27 pF, 50 kOhm	7 GHz, 0.44 pF, 25 kOhm

Used with 1168A or 1169A probe amplifier, the E2677A differential solder-in probe head provides 10 GHz and 12 GHz bandwidth respectively.

17 Common Error Messages

When performing DDR3 tests, error message dialog boxes can occur due to improper configuration settings. This section describes the common errors, causes and solution to the problem.

Required Triggering Condition Not Met

The following error message will appear when a time-out occurs. This error message indicates that the required triggering condition is not met. This is followed by test cancellation and aborting message. All pending tests will be cancelled.

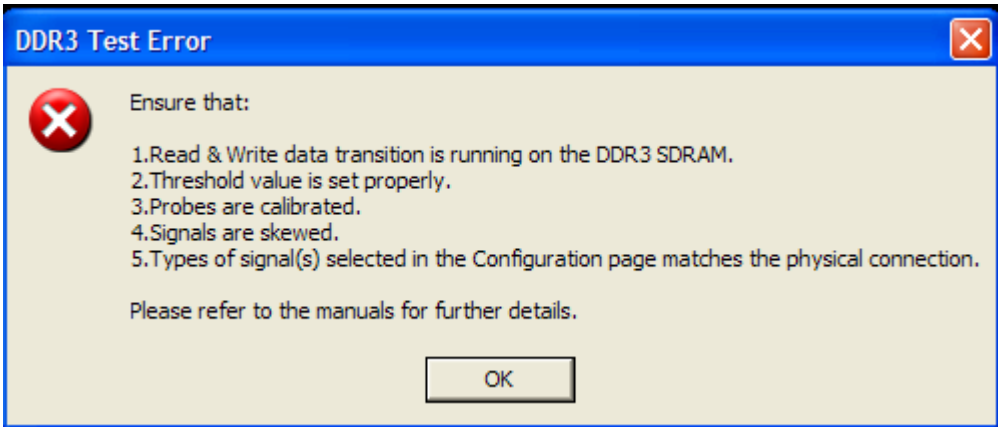


Figure 106 Required Trigger Condition Not Met Error Message

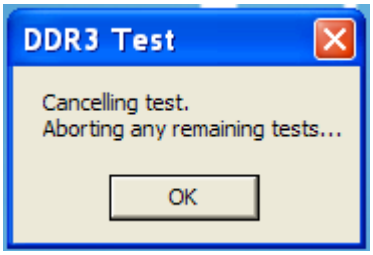


Figure 107 Cancel and Abort Test Message

These error dialog boxes appear when one of the following configuration errors is encountered.

- Required triggering condition is not met. For example, if the setup time condition in a triggering requirement, is not met within a certain time (approximately 10s), the time-out error will occur.
- Attempt to run the Electrical tests without first executing the RAM reliability test software on the DDR3 Device Under Test (DUT) system.
- Attempt to run the Electrical tests without providing any test signal to the oscilloscope.
- Threshold value is not properly set.
- Signals are not skewed.

- The type of signals selected in the Configuration page does not match the physical connection.

Ensure that:

- The RAM reliability test software is running to exercise the SDRAM. This ensures that there are Read and Write signals running on the SDRAM in order for the application to capture the signal.
- The threshold is properly set according to the actual signal performance. For example, if the maximum voltage of the DQ signal is 1.8V and the minimum voltage is 40mV, you must ensure that the upper and lower threshold value does not exceed the minimum and maximum limit, in order to trigger the signal. Scope will not be triggered if the upper threshold is set to be above 1.8V, since the maximum voltage on the actual signal is just 1.8V and below.
- The probes are properly calibrated and skewed. Ensure that correct probes are used and they are properly calibrated, so that it reflects the actual signal and is not over or under amplified. Similarly, ensure that the channels are properly soldered on the DDR module and ensure that the signals are not over skewed.
- The types of signals selected in the Configuration page matches the physical connection. For example, if Channel 1 is physically connected to the Clock signal, ensure that you select the same in the Configuration page.

Software License Error

When you load the U7231A DDR3 Compliance Test Application, it checks for the required software licenses. When one of the optional licenses is not detected, the application will limit the available test options and the Set Up tab will look similar to following screenshot.

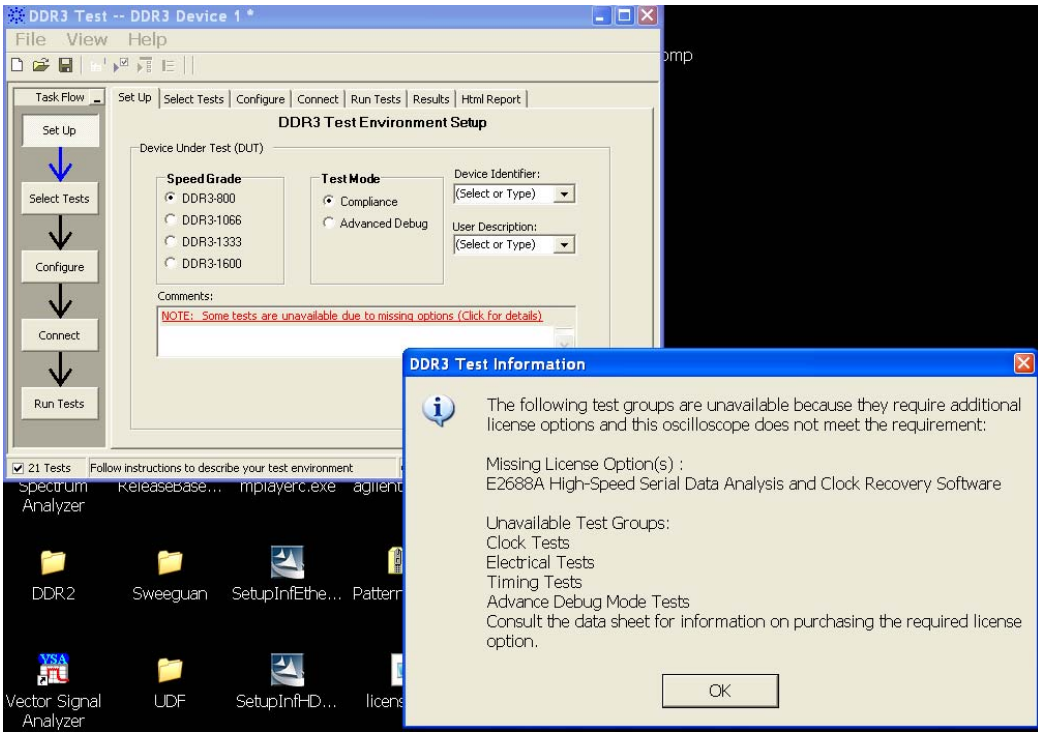


Figure 108 Software License Error

Ensure you have installed all required licenses before running the U7231A DDR3 Compliance Test Application.

Frequency Out of Range Error

You are allowed to type in the DUT data rate for the Advanced Debug Mode tests. However, if you enter an incorrect data strobe test signal frequency, the following error dialog box appears. For example, if the selected DDR3 speed grade option is DDR3-800, the expected frequency of the data strobe signal, DQS is 400MH (half of the data transfer rate). However, if the measured DQS frequency is out by +/-10% of the expected frequency value, exception will be thrown.

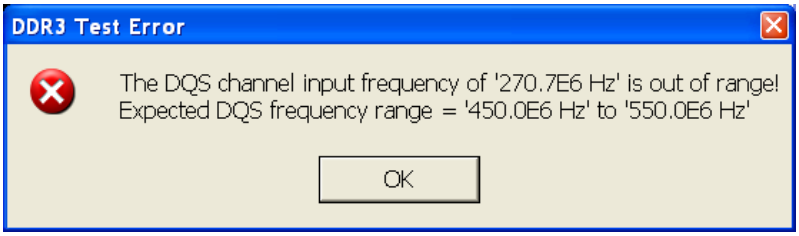


Figure 109 Frequency Out of Range Error

Type in the correct data rate, within the range, as mentioned in the error message box.

Invalid Test Mask Error

Selecting Advanced Debug as the Test Mode shows you an additional command button - **Set Mask File**. You need to select a valid test mask that can by recognized by the oscilloscope.

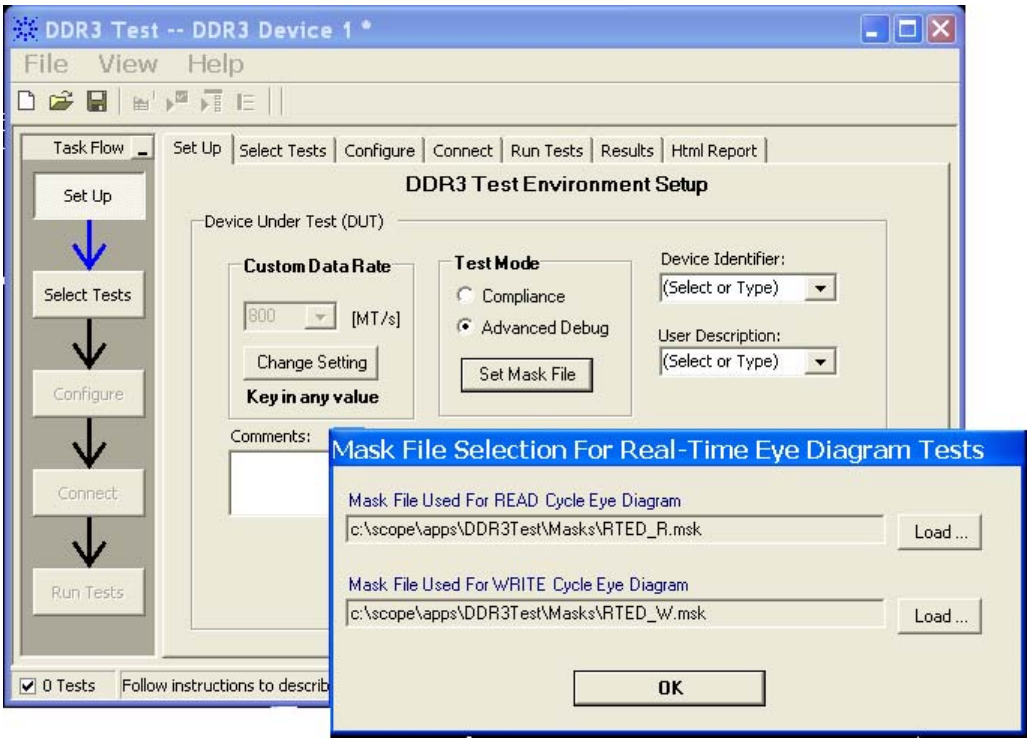


Figure 110 Selecting Mask File for Eye Diagram Tests

Attempt to load an invalid test mask will prompt you with the following error message.

Figure 111 Selecting Mask File for Eye Diagram Tests

Missing Signal Error

This error occurs when the required signals are either not selected in the “Channel Setting” configuration or not connected to the oscilloscope. Ensure that correct channel is selected based on the signal that is physically present at the oscilloscope channel.

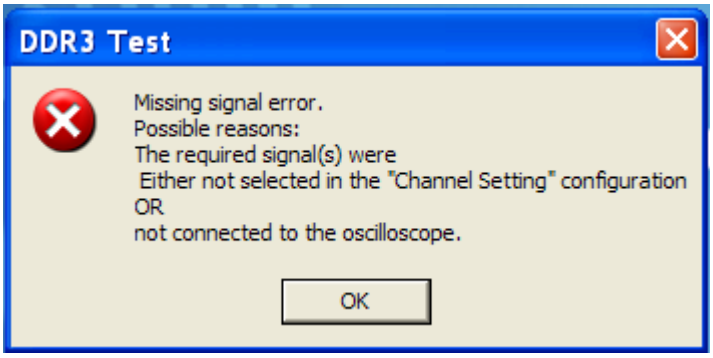


Figure 112 Missing Signal Error Message

Invalid Pre/PostAmble Signal Error

This error occurs during the multiple trial run if there is no significant voltage level transits when the driver is turned on or off during the preamble or postamble. You should verify the signals especially the DQS and DQ if they provide a valid preamble or postamble signal. If there is no significant voltage level transition when the driver is turned on or off during the pre-amble OR post-amble, the system will throw an exception to prompt user to verify the signal.

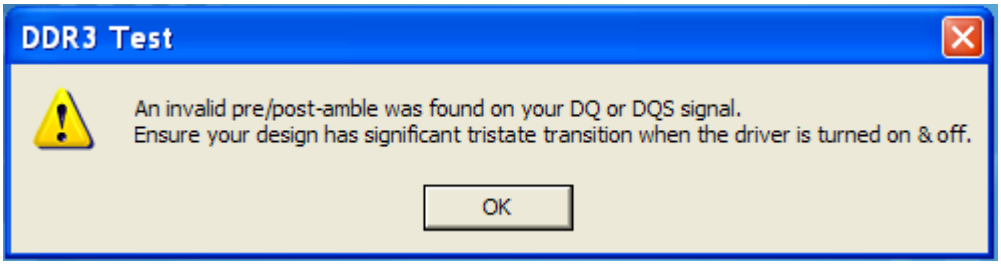


Figure 113 Invalid Pre/Post Amble Signal Error Message

You can disable this error message at the Configure tab. Turn the “Signal error message prompt” to the Disable mode. This will prevent the above error message being prompt during the multiple trial run.

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